PRATHYUSHA ENGINEERING COLLEGE

POONAMALLEE-TIRUVALLUR HIGH ROAD, CHENNAI–602 025

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

IV SEMESTER

EC8453 – LINEAR INTEGRATED CIRCUITS

Regulation – 2017

Academic Year 2019 – 20

UNIT 1- BASICS OF OPERATIONAL AMPLIFIERS		
PART-A		
Q.No	**Questions**	**BLOOMS TAXANOMY LEVEL**
1.	Outline the importance of offset voltage of an operational amplifier?	LOW
2.	Define CMRR.	LOW
3.	Mention the importance of current mirror circuit used in differential amplifier stages.	MEDIUM
4.	Specify the ideal characteristics of Op-amp and methods can be used to produce voltage sources.	LOW
5.	How will you MEDIUM the term 'thermal drift'?	LOW
6.	Write short note about current mirror with magnification.	LOW
7.	Define slew rate and what causes the slew rate?	LOW
8.	State loading effect? How can you reduce it?	MEDIUM
9.	Why do we use R_{comp} resistor?	MEDIUM
10.	What is the gain cross over and phase cross over frequencies?	MEDIUM
11.	Categorize the characteristics of Non-ideal op-amp.	HIGH
12.	Develop the internal block diagram of an Op-amp.	HIGH
13.	Illustrate the pin diagram of IC 741.	HIGH
14.	Examine the importance of input off set current.	HIGH
15.	Analyze about input bias current.	HIGH
16.	Inspect the draw backs of using large R_C in differential amplifier.	HIGH
17.	Brief the necessity of active loads preferred than passive loads in the input stage of an operational amplifier.	MEDIUM
18.	Justify that, why IC741 op-amp not used for high frequency applications?	MEDIUM

19.	Calculate the maximum distorted amplitude that a sine wave input of 10 kHz, can produce at the output of an op-amp whose slew-rate is 0.5v/μsec.	HIGH
20.	A Differential amplifier has a differential voltage gain of 2000 and common mode gain of 0.2. Determine CMRR.	HIGH

PART-B

S.NO	QUESTIONS	MARKS	BLOOMS TAXANOMY LEVEL
1.	Define and explain slew rate. Derive its equation. Also explain method adapted to improving slew rate.	(13)	LOW
2.	(i) Write down the characteristics and their respective values of an ideal operational amplifier. (ii) Draw the circuit of basic current mirror and explain its operation.	(6) (7)	LOW
3.	(i) Describe about output offset voltage. Explain methods to nullify offset voltage. (ii) With neat circuit diagram, explain the operation of voltage reference circuit using temperature compensation.	(7) (6)	LOW
4.	(i) Discuss on current mirror with magnification. (ii) Use appropriate block diagram, explain the general stages of an Op-Amp IC.	(6) (7)	MEDIUM
5.	(i) What is input and output voltage and current offset? How are they compensated? (ii) With a neat diagram derive the AC performance close loop characteristics of Op-amp to discuss on the circuit Bandwidth, Frequency response and slew rate.	(7) (6)	MEDIUM
6.	(i) Draw the circuit of basic current mirror and explain its operation.	(6)	HIGH

	(ii) Give the detail the DC analysis of a basic differential amplifier.	(7)	
7.	Obtain the expression for differential gain, common mode gain, CMRR, R_I and R_O of an emitter coupled differential amplifier.	(13)	HIGH
8.	(i) Sketch the Wilson current source and give short note about it. (ii) Using suitable diagram and necessary equations, explain the concept of Widlar current source used in op-amp circuit.	(5) (8)	HIGH HIGH
9.	Show the transfer characteristics of dual input differential amplifier showing the linear and limiting regions. Comment on the same.	(13)	MEDIUM
10.	(i) Derive the functional parameters for an inverting mode negative feedback gain circuit with a 741op-amp in IC inverting mode, with R1=1Kohm, Rf=40Kohm and compute Af, Rif, Rof, BW, offset voltage. (ii) Discuss briefly on the differential mode Instrumentation amplifier.	(7) (6)	HIGH HIGH
11.	Examine the working principle of BJT differential amplifier with active load.	(13)	MEDIUM
12.	(i) Compose the concept of Widlar current source used in op-amp circuit with suitable circuit diagram and necessary equations. (ii) Justify the preference of active load over passive load.	(10) (3)	HIGH
13.	Write note about LF155 JFET input operational amplifier and TL082 wide bandwidth dual JFET input operational amplifier with necessary diagram.	(13)	LOW
14.	State and explain about CMRR, A_d, A_c and suggest a method to improve CMRR.	(13)	HIGH

PART-C			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1	Derive the transfer characteristics of dual input differential amplifier showing the linear and limiting regions. Comment on the same.	(15)	HIGH
2	(i) A square wave peak-to-peak amplitude of 50mV has to be amplified to a peak-to-peak amplitude of 3V, with rise time of 4 μs or less. Can IC741 be used? (ii) A IC741 Op-Amp whose slew rate is 0.5V/μs is used as an inverting amplifier with a gain of 50.The voltage gain Vs	(5) (10)	HIGH

	frequency curve of IC741 is flat up to 20 kHz. What maximum peak to peak input signal can be applied without distorting the output?		
3	Explain in detail the A.C analysis of dual input, balanced output differential amplifier or derive the expression for differential gain, common mode gain, CMRR, R_I and R_O of an emitter coupled differential amplifier.	(15)	HIGH
4	Illustrate each direct current characteristics of operational amplifier with necessary equations and diagrams.	(15)	HIGH

UNIT 2- APPLICATIONS OF OPERATIONAL AMPLIFIERS		
Q.No	**Questions**	**BLOOMS TAXANOMY LEVEL**
1.	Mention the advantages of variable trans conductance technique?	LOW
2.	Write the other name for Clipper circuit?	LOW
3.	What is the need for converting a first order filter into a second order filter?	LOW
4.	How is the current characteristic of a PN junction employed in a log amplifier?	LOW
5.	Compare the performance of inverting and non-inverting operational amplifier configurations.	LOW
6.	Give the applications of inverting & non- inverting amplifiers.	LOW
7.	Draw the inverting & non- inverting amplifiers with appropriate equations.	LOW
8.	List the applications for each of the following circuits: Voltage follower, Peak detector, Schmitt trigger, Clamper.	MEDIUM
9.	Why integrators are preferred over differentiators in analog computers?	MEDIUM
10.	Summarize the frequency expressions for LPF, HPF and BPF.	MEDIUM
11.	Enumerate the advantages & disadvantages of passive filters?	HIGH
12.	Sketch the opamp integrator & differentiator circuit with necessary equation.	HIGH

13.	Define comparator and function of a phase shift circuit ?	HIGH
14.	Illustrate some of the important features of an instrumentation amplifier.	HIGH
15.	Construct an adder circuit using op-amp to get the output expression as Vo = - (0.1V1 +V2+5V3)	HIGH
16.	Demonstrate the need for frequency compensation in practical op-amps	HIGH
17.	Show the necessity of active guard drive in an instrumentation amplifier.	MEDIUM
18.	Find the output voltage of the following circuit. Given R1 =R2 = 10kΩ and Rf = 100	MEDIUM
19.	How does precision rectifier differ from the conventional rectifier?	HIGH
20.	Design an amplifier with a gain of -10 and input resistance equal to 10 kΩ.	HIGH

PART-B

S.NO	QUESTIONS	MARKS	BLOOMS TAXANOMY LEVEL
1.	(i) With a suitable circuit diagram, explain the operating principle of an instrumentation amplifier and derive its gain. (ii) Design a second order Butterworth low-pass filter having upper cut-off frequency of 2.1961 kHz	(7) (6)	LOW
2	Compare and contrast Adder, Subtractor, and Averaging circuit using op-amp with equations.	(13)	
3.	Illustrate the operation of current to voltage and Voltage to current converter circuits.	(13)	LOW
4.	With neat figures describe the circuit using op-amps on the following of (i) Integrator and double integrator circuit (ii) First order High pass filter	(7)	MEDIUM
5.	Derive the expression for log computation using op-amp and explain necessary circuit diagram.		MEDIUM

6.	With neat figures describe the circuit using op-amps on the following of (i) Integrator and double integrator circuit (ii) First order High pass filter		HIGH
7.	Draw and explain the circuit of a voltage to current converter if the load is i) Floating ii) Grounded	(7) (6)	HIGH
8.	(i) Design an OP-AMP based first order active low pass filter. (ii) Creating a second order Butterworth LPF having upper cut-off frequency 1 kHz. Determine the frequency response.	(8) (5)	HIGH HIGH
9.	i) Analyze the distinct features of the precision diode. ii) Using appropriate equations discuss about the working of Half wave Precision Rectifier.	(3) (10)	MEDIUM
10.	(i) With neat sketch explain the working of Full wave Precision Rectifier in detail. ii)Sketch the Integrator circuit and explain the working principle	(8) (5)	HIGH HIGH
11.	i) With neat diagram explain the operation of Schmitt trigger. ii) Give detailed note about op-amp band pass filter.	(5) (8)	MEDIUM
12.	Conclude that how antilog computations are performed using IC-741 explain using circuits and necessary equations.	(13)	HIGH
13.	(i) Examine the principal of operation of Voltage follower with the neat circuit diagram and mathematical expressions. (ii) With the neat circuit diagram and mathematical expressions, explain the operation of Scale changer.	(6) (7)	HIGH

PART-C			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1	Evaluate Inverting adder and Non-inverting adder with neat circuit diagram and mathematical expressions.	(15)	HIGH
2	Create any of three op-amp based mathematical function circuits	(15)	HIGH
3	i) Design a Butterworth low pass filter circuit using operational amplifier.	(15)	HIGH

	ii) Design a wide band filter having FL=400Hz, FH=2kHz and pass band gain of 4.Find the value of Q of filter.		
4	Justify that how the circuit using Op-amps on the operation of. (i) Zerocross Detector, Clipper and Clamper circuit (ii) Scmitt Trigger.	(8) (7)	HIGH

UNIT 3-ANALOG MULTIPLIER AND PLL		
PART-A		
S.NO	**QUESTIONS**	**BLOOMS TAXANOMY LEVEL**
1	Outline the basic building blocks of PLL.	LOW
2	Define capture range and lock range of PLL.	LOW
3	What is Pull-in time?	LOW
4	For perfect lock, what should be the phase relation between the incoming signal and VCO output signal?	HIGH
5	Mention the classification of phase detector. Write about switch type phase detector.	MEDIUM
6	Illustrate the problems associated with switch type phase detector	MEDIUM
7	Why VCO is also called as V to F converter?	LOW
8	On what parameters does the free running frequency of VCO depend on?	MEDIUM
9	Give the expression for the VCO free running frequency.	MEDIUM
10	Demonstrate Voltage to Frequency conversion factor.	MEDIUM
11	Develop the purpose of having a low pass filter in PLL.	MEDIUM
12	Discuss the effect of having large capture range.	HIGH
13	Estimate that the frequency stability obtained in a PLL by use of VCO.	HIGH
14	How are square root and square of a signal obtained with multiplier circuit?	LOW
15	Identify the merits of companding	MEDIUM
16	List out the applications of OTA.	LOW
17	Asses the need of pre-distortion circuits in Gilbert analog multiplier and how is the configuration of Gilbert multiplier done with pre-distortion circuits.	HIGH
18	Analyze the necessity of modulation.	HIGH
19	Develop the circuit of AM detector using PLL.	HIGH

20	Distinguish the advantages & disadvantages of monolithic PLLs over Discrete PLLs.	HIGH

PART-B			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1.	How would you describe the block diagram of PLL and derive the expression for Lock range and capture range.	(13)	MEDIUM
2.	Illustrate the operation of VCO with neat block diagram. Also derive an expression for f_0.	(13)	HIGH
3.	(i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (ii) Identify how a frequency doubler can be realized using this cell.	(8) (5)	HIGH
4.	Discuss any three applications of PLL in detail .	(13)	MEDIUM
5.	(i) Estimate the working principle of operational Transconductance Amplifier (OTA). (ii) Explain the application of VCO for FM generation. (5)	(8) (5)	MEDIUM
6	(i) Define capture range and lock range. (ii) Explain the process of capturing the lock and also derive for capturerange and lock range.	(3) (10)	LOW MEDIUM
7.	(i) How would you explain the working of a VCO? (ii) Derive the expression for voltage to frequency conversion factor.	(6) (7)	LOW HIGH
8.	Determine how the IC 565 PLL can be used as a Frequency multiplier/divider.	(13)	HIGH
9.	(i) Examine the multiplier cell using emitter-coupled transistor pair. (ii) Analyze that the output voltage is proportional to the product of the two input voltages and state their limitations.	(8) (5)	HIGH
10.	Briefly explain the use of PLL for FM detection and the process of FSK demodulation.	(8)	HIGH
	Discuss the following applications of Analog Multiplier ICs (i) Voltage squarer (ii) voltage divider (iii) square rooter (iv) Phase angle detector	(13)	MEDIUM
11.	(i) For PLL 565, given the free-running frequency as 100KHz, the demodulation capacitor of 2μf and supply voltage is ±6V, determine the lock and capture frequencies and identify the component values.	(8)	HIGH

	(ii) A PLL has a free running frequency of 300KHz and the bandwidth of the low pass filter is 50KHz. Check whether the loop acquires lock for an input signal of 320KHz.	(5)	
PART-C			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1	(i)Discuss the basic analog multiplication techniques. (ii)Develop the expression for free running frequency of voltage controlled oscillator.	(7) (8)	MEDIUM
2	Explain the operation of a variable trans conductance multiplier circuit. Derive the expression for its output voltage.	(15)	HIGH
3	Measure the closed loop analysis of PLL with necessary diagrams.	(15)	HIGH
4	Construct the block diagram and explain principle of working, characteristics and applications of: (i) Frequency synthesizer. (ii) Frequency shift keying (FSK) Demodulator	(7) (8)	HIGH

UNIT 4-ADC & DAC		
PART-A		
S.NO	**QUESTIONS**	**BLOOMS TAXANOMY LEVEL**
1	What is the function of integrating type converter? List out some integrating type converters.	LOW
2	Review the principle of operation of successive Approximation ADC.	MEDIUM
3	Cite the main advantages of integrating type ADCs.	LOW
4	Define Sampling .	LOW
5	Compare the advantages and drawbacks of a dual-slop ADC.	MEDIUM
6	Distinguish between conversion time and settling time.	HIGH
7	Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values.	MEDIUM
8	Give the advantages of inverted R-2R (current type) ladder D?A converter over R -2R(voltage type) D/A converter ?	LOW

9	Brief the need for electronic switches in D/A converter and mention the names of the switches used in MOS transistors.	LOW
10	Summarize delta modulation.	MEDIUM
11	How would you justify which type of ADC is the fastest?	MEDIUM
12	Outline the principle of operation of voltage to time conversion.	LOW
13	Calculate the values of LSB and MSB for an 8-bit DAC for 0V to 10V range.	HIGH
14	Interpret the features of granular error and slope overload error.	MEDIUM
15	An 8 bit A/D converter accepts an input voltage signal of range 0 to 12v. What is the digital output for an input voltage of 6V?	MEDIUM
16	Evaluate the number of comparators required for realizing a 4-bit flash ADC.	HIGH
17	Compare and contrast binary weighted and R-2R ladder DAC.	HIGH
	Identify the need of Sample and hold circuit and Why schottky diodes are used in sample and hold circuits?	MEDIUM

PART-B

S.NO	QUESTIONS	MARKS	BLOOMS TAXANOMY LEVEL
1	i) How would you categorize A/D converters? ii) Discuss the working principle of successive approximationtype ADC.	(6) (7)	LOW
2	i) Estimate the working of R-2R ladder type DAC. ii) Compare binary weighted DAC with R-2R ladder network DAC.	(7) (6)	HIGH
3	i) With circuit schematic explain analog switches using FET. ii) What is meant by resolution, offset error in ADC.	(7) (6)	LOW
4	i) Explain in detail on the operational features of 4-bit weighted resistor type D/A converter. ii) Differentiate between current mode and voltage mode R-2Rladder D/A converters.	(7) (6)	HIGH
5	Show the operation of any two direct type of ADCs and Explain.	(13)	LOW
6	Summarize the following Digital to Analog & Analog to Digital conversion techniques. (i)Flash type ADC (ii)Weighted resistor DAC	 (7) (6)	LOW
7	Draw the diagram of sample and hold circuit. State how you will reduce its hold mode droop.	(6) (7)	LOW
8	Design a 4–bit binary weighted resistor DAC for the following specifications: Use LM741 op-amp, R = 10kΩ, Vref	(13)	HIGH

	=2.5V and full scale output = 5V.		
9	A dual slope ADC has a full scale input of 2 Volts .It uses an integrating time of 10ms and integrating capacitor of 0.1μf.the maximum magnitude of the integrator output should not exceed 3V. Calculate the value of the integrating resistor.	(13)	MEDIUM
10	Describe in detail about the single slope type ADC with neat sketch.	(13)	MEDIUM
11	i) Sketch the block diagram and explain the working of Charge Balancing VFCS ii) With functional block diagram explain A/D converter using Voltage to Time converter with input and output waveforms.	(6) (7)	HIGH
12	i) Elaborate the operation of high speed sample and hold circuits. ii) Develop a system employs a 16-bit word for representing the input signal. If the maximum output voltage is set 2V,calculate the resolution of the system and its dynamic range.	(9) (4)	LOW
13	i) Summarise the various important specifications of both D/A and A/D converters generally specified by the manufactures are analysed. ii) A 8-bit A/D converter accepts an input voltage signal of range 0 to 9V, What is the minimum value of the input voltage required for generating a change of 1 least significant bit ? specify the digital output for an input voltage of 4 V. What input voltage will generate all 1s at the A/D converter output?	(7) (6)	HIGH

PART-C			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1	i) For a 4-bit R-2R ladder D/A converter assume that the full scale voltage is 16V.Calculate the step change in output voltage on input varying from 01111 to 1111. ii) Discuss the important specification of Data Converters.	(10) (5)	HIGH
2	i) Compare single slope ADC and dual slope ADC. ii) Draw the circuit and explain the working of dual slope A/D converter. iii) Calculate t_2 for a particular dual slope ADC, t_1 is 83.33ms and the reference voltage is 100mv if 1. V_1 is 100 mv and 2. 200 mv	(3) (7) (5)	HIGH

3	Design the R-2R 4-bit converter and assume that feedback resistance R_f of the op-amp is variable, the resistance R=10kΩ and V_R =10V. Determine the value of R_f that should be connected to achieve the following output conditions. (i) The value of 1 LSB at the output is 0.5V (ii) An analog output of 6V for a binary input of 1000. (iii) The Full-scale output voltage of 12V The actual maximum output voltage of 10V	(15)	HIGH

UNIT 5-WAVEFORM GENERATORS AND SPECIAL FUNCTION ICSG		
PART-A		
S.NO	**QUESTIONS**	**BLOOMS TAXANOMY LEVEL**
1	What is the need for voltage regulator ICs?	LOW
2	List the characteristics and applications of Opto coupler.	MEDIUM
3	Sketch a fixed voltage regulator circuit and state its operation.	LOW
4	Give the conditions for oscillation.	LOW
5	What is a switching regulator?	MEDIUM
6	List the applications of 555 timer in Monostable mode of operation.	HIGH
7	Classify the three different wave forms generated by ICL8038.	MEDIUM
8	Mention the need for current limiting in voltage regulators.	LOW
9	Compare Linear regulator and Switched mode regulator.	LOW
10	Mention the function of a voltage regulator .Give some examples of monolithic IC voltage regulators.	MEDIUM
11	Draw the functional block diagram of IC 723 regulator.	MEDIUM
12	Compare the principle of linear regulator and a switched mode power supply.	LOW
13	How would you classify an opto-coupler , also mention the current transfer ratio of an opto coupler.	HIGH
14	Define line and load regulation of a regulator.	MEDIUM
15	In a Astable multivibrator of 555 times R_A=606kΩ and C=0.1μF. Calculate (a) t_{HIGH} (b)t_{LOW} (c) free running frequency (d) duty cycle (D).	MEDIUM
16	How does switched capacitor emulate resistor?	HIGH
17	With reference to a VCO, define voltage to frequency conversion factor K_v.	HIGH

18	In a monostable multivibrator using 555 timer, R=100kΩ and the time delay is 100ms.Find the value of C.	MEDIUM
19	List the types of Multivibrator.	LOW
20	Give reasons for the purpose of connecting a capacitor at the input and output side of an IC voltage regulator?	LOW

PART-B			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1	Write a short notes on (i) Opto couplers (ii) Switched capacitor filter (iii)Audio power amplifier	(10) (5)	HIGH
2	Demonstrate and explain the functional diagram of LM 380 power amplifier.	(3) (7) (5)	HIGH
3	Illustrate the essential characteristics of power amplifier.	(8)	LOW
4	What is 555 timer? Explain the working of 555 timer as Monostable Multivibrator.	(7)	HIGH
5	Derive an expression for the frequency of oscillation with relevant waveforms.	(6)	MEDIUM
6	Analyze and explain the operation of switching regulator with neat diagram.	(8)	MEDIUM
7	Examine the operation of frequency to voltage converters.	(6)	HIGH
8	Show the working of Astable Multivibrator using op-amp.	(7)	LOW
9	Outline any one application of Astable Multivibrator in detail.	(13)	HIGH
10	Design a phase shift oscillator to oscillate at 100 Hz.	(7)	HIGH
11	Design a frequency to voltage converter using IC VFC 32 for a full scale output of 8V for a full scale input frequency of 80kHz with a maximum ripple of 8mV.	(13)	HIGH
12	Define voltage regulator and explain the working of Linear Voltage regulator with neat circuit diagram using op-amps. List any two important features of linear voltage regulator IC723.	(7)	MEDIUM
13	Assess the working principle of monolithic switching regulator.	(7)	MEDIUM
14	Evaluate how the frequency is computed using voltage to frequency converter.	(8)	HIGH

15	With neat diagram, explain the operation of an astable and monostable multivibrators using opamp. Illustrate the functional diagram and connection diagram of a low voltage regulator and explain.	(13)	LOW
16	i) Develop the basic principle of function generator? Draw the schematic of ICL 8038 function generator and discuss its features. ii) Solve the expression for the frequency of a triangular waveform generator and explain the circuit.	(13)	HIGH
17	i) Describe the 555 timer IC.design a astable multivibrator circuit to generate output pulses of 25%,50% duty cycle using a 555 timer IC with the choice of C=0.01μF and a frequency of 4 kHz. ii) Demonstrate Monostable multivibrator with necessary diagrams and derive for ON time and recovery time.	(13)	HIGH
18	Interpret the working of monostable multivibrator.	(13)	HIGH
19	Analyzing the working of a general purpose voltage regulator.	(7)	MEDIUM
20	Justify the need for isolation amplifiers.	(6)	MEDIUM

PART-C			
S.NO	**QUESTIONS**	**MARKS**	**BLOOMS TAXANOMY LEVEL**
1	i) In a astable multivibrator using 555 timer Ra=6.8K,Rb = 3.3K, C=0.1uF.Calculate the free running frequency. ii) Design a square wave generator using 555timer for a frequency of 120Hz and 60% duty cycle. Assume C=0.2uF.	(8) (7)	HIGH
2	i) Analyze the important features and pin details of switched capacitor filter IC MF10. ii) Design a wave generator using 555 timer for a frequency of 110Hz and 80 % duty cycle. Assume C =0.12μF	(8) (7)	HIGH
3	Derive the expression and circuit operation for LM 380 Audio power amplifier.	(15)	HIGH
4	Design an adjustable voltage regulator circuit using LM 317 for the following specifications: Input dc voltage =13.5 V; Output dc voltage = 5 to 9V; Load current (maximum) = 1A.	(15)	HIGH