EC8392 DIGITAL ELECTRONICS
QUESTION BANK

UNIT I   DIGITAL FUNDAMENTALS

PART-A

1. State Demorgn's theorem.

2. Simplify the following Boolean expression XY+X(Y+Z)+Y(Y+Z).

3. Show how to connect NAND gates to get an AND gate and OR gate.

4. Define the laws of Boolean algebra.

5. For a switching function of 'n' variables, how many distinct minterms and maxterms are possible?

6. Define canonical form.

7. State the absorption properties of Boolean algebra.

8. Simplify the Boolean Expression F= A+AB

9. Show that NAND connection is not associative.

10. Design XOR gate using NAND gate.

11. Design XNOR gate using NOR gates.

12. Define minterm and maxterm.

13. What is K-map?

14. Which gates are called as the universal gates?

15. What are called don't care conditions?

16. What is tabulation method?

17. State the limitations of karnaugh map.

18. What is a prime implicant?

19. What is an essential prime implicant?

20. List out the advantages and disadvantages of K-map method?

21. List out the advantages and disadvantages of Quine-Mc Cluskey method?

22. State De morgan theorem.

23. Express the function in to canonical form Y=A+B'C.

24. Convert $(10.25)_{10}$ = ( )$_2$

25. Convert $(11101001110)_2$= ( )$_8$

26. Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method. Subtract by direct method also and compare.

27. Find the complement of F=wx+yz and then show that FF'=0.

28. What is the largest number that can be expressed with 14 bits? Determine the equivalent decimal and hexadecimal numbers.

PART-B

1. Simplify the following Boolean function F, using Quine Mccluskey method and verify the result using K-Map F(A,B,C,D)= $\sum m(1,3,5,8,9,11,15)+d(2,13)$

2. Minimize the following logic function using K-Map and realize using NAND and NOR gates.
   F(A,B,C,D,E)=$\sum m(0,1,4,5,9,11,13,15,16,17,25,27,28,29,31)+d(20,21,22,30)$

3. Implement Y=AB+A+(B+C) using NAND gates only

4. Explain about Boolean postulates and laws.

5. Simplify the following Boolean function F, using Quine Mccluskey method and verify the result using K-Map F(A,B,C,D)=$\sum m(1,2,3,7,8,9,10,11,14,15)$

6. Simplify using K-Map A'B'C'D'+A'CD'+AB'D'+ABCD+A'BD

7. Simplify the function in SOP and POS using K-Map

   F(A,B,C,D,E)=$\sum m(0,1,3,4,5,9,11,12,13,15)$

8. Implement the basic gates using Universal gates.

9. Simplify the following Boolean function F, using Quine Mccluskey method and verify the result using K-Map F(A,B,C,D)= M(0,3,5,9,11)+d(4,10,15)

UNIT II   COMBINATIONAL CIRCUIT DESIGN

PART-A

1. Convert a decoder into a demultiplexer.

2. Give the logical expression for sum output and carry output of a full adder.

3. Write the design procedure for combinational circuits.

4. Construct a 4-bit parallel adder/substractor using Full adders and XOR gates.

5. How logic circuits of a digital system are classified?

6. Explain how parity can be used for error detection.

7. What is an encoder and decoder?

8. Compare combinational circuit and sequential circuit.

9. What is data selector? (Or) Define Multiplexer.

10. What is data distributor (Or) Define demultiplexer.

11. What is priority encoder?

12. What is combinational circuit?

13. Define magnitude comparator.

14. What is Half adder?

15. What is Full adder?

16. What is Binary adder?

18. What is Half subtractor?

19. What is BCD adder?

20. What is Parity generator and parity checker?

21. What is code converter?

22. Give the applications of Demultiplexer.

23. List out the applications of decoder?

24. List out the applications of Mux.

25. List out the applications of comparators?

26. What is carry look-ahead addition? Why it is called as fast adder?

27. Distinguish between Decoder & Demux.

28. Design full adder using half sdder.

29. Compare serial adder and parallel adder.

30. Design 2-bit comparator.

PART-B

1. With a neat diagram, explain in detail about the working of a 4 bit look ahead adder. Also mention its advantages over conventional adder.

2. Design 4 bit decimal adder using 4 bit binary adders.

3. Design a 4-bit magnitude comparator with three outputs : A>B, A=B, A<B

4. Design a 4:1 multiplexer circuit.

5. Implement the following Boolean function using 8:1 multiplexer

   $F(A,B,C,D)= \sum m(0,1,3,4,7,8,9,12,15)$

6. Design a combinational circuit that accepts a 4 bit binary number and generates an output binary number equal to the square of the number.

7. Explain the operation of four input priority encoder.

8. Design a 5X32 decoder using 3X8 decoder and summarize how many decoders are required?

9. Design BCD to Excess-3 code converter and draw the logic diagram.

10. Design 4-bit binary adder/substractor.

11. Design BCD to grey code converter and draw the logic diagram.

12. Design 2-bit binary multiplier.

13. Design 3-bit parity checker and parity generator circuit.

14. Design full adder using decoder.

UNIT III   SYNCHRONOUS SEQUENTIAL CIRCUITS

PART-A

1. Differentiate between edge triggering and level triggering.

2. How a D Flip flop is converted in to T flip flop.

3. Derive the characteristic equation of D flip flop.

4. Realize JK flip flop.

5. What is a sequential circuit? Give an example.

6. Distinguish between synchronous counter and asynchronous counter.

7. Define clocked sequential circuit.

8. Distinguish between latch and flip-flop.

9. Why D latch is called transparent latch.

10. What is triggering?

11. What is meant by the term "edge triggered"?

12. Define set up time.

13. Define hold time.

14. Define propagation delay time.

15. Define the term preset and clear/Reset in flip-flop.

16. What is state equation?

17. What is state table?

18. What is state diagram?

19. What are Mealy and Moore machines?

20. What is meant by the term state-reduction?

21. Write the procedure for designing asynchronous sequential circuit.

22. Write the flip-flop excitation tables for JK and T FF.

23. What is register?

24. What is counter?

25. What is a shift register?

26. Define unidirectional, bidirectional and universal shift register.

27. Define binary counter.

28. Define binary count-down counter.

29. What is decade counter?

30. What is modulo-N counter (divide-by-N counter)?

31. Define a ring counter.

32. What is Johnson counter?

33. When is counter said to suffer from lock out?

34. What are the states of a 4-bit ring counter?

35. How a latch can modify to form a flip-flop?

36. What is a sequence generator?

37. What is Flip-flop? And mention its types?

38. What is latch?

39. Define race around condition.

40. What is a master-slave flip-flop?

41. Define rise time.

42. Define fall time

43. Define skew and clock skew.

44. Applications of Flip-Flop.

PART-B

1. Explain the operation of MOD-6 counter.

2. Explain about triggering of flip flops

3. Using SR Flip Flop design a parallel counter which counts the sequence
   000,111,101,110,001,010,000,…….

4. A clocked sequential circuit with single input x and single output z produces output z=1,
   whenever the input x completes the sequence 1011 and overlapping is allowed:

   i) Obtain the state diagram

   ii) Obtain its minimum state table and design circuit with D flip flops

5. Explain the operation of SISO,SIPO, PISO and PIPO.

6. Design a 4-bit binary counter and explain its counting process. Discuss how to use this circuit to
   perform both up and down counting.

7. With neat logic diagram and function table, explain the working of a SR flip flop

8. Using T Flip-flop design binary counter which counts in the sequence 000, 001,

010, 011, 100, 101, 110, 111, 000

9. Explain about Bi directional and universal shift registers.

10. Explain 3-bit synchronous up/down counter.

11. Explain 4-bit ring counter using D-Flip fliop.

12. Explain 4-bit jhonson counter.

13. Explain about master slave JK flip flop.

14. Explain in detail about moore and melay circuits.

15. Design 4-bit Asynchronous counter using JK flip flop with its timing diagram

16. Realize JK Flip flop using SR Flip flop and derive their characteristics equations

17. Realize T Flip flop using only NAND gates and derive the characteristic equation.
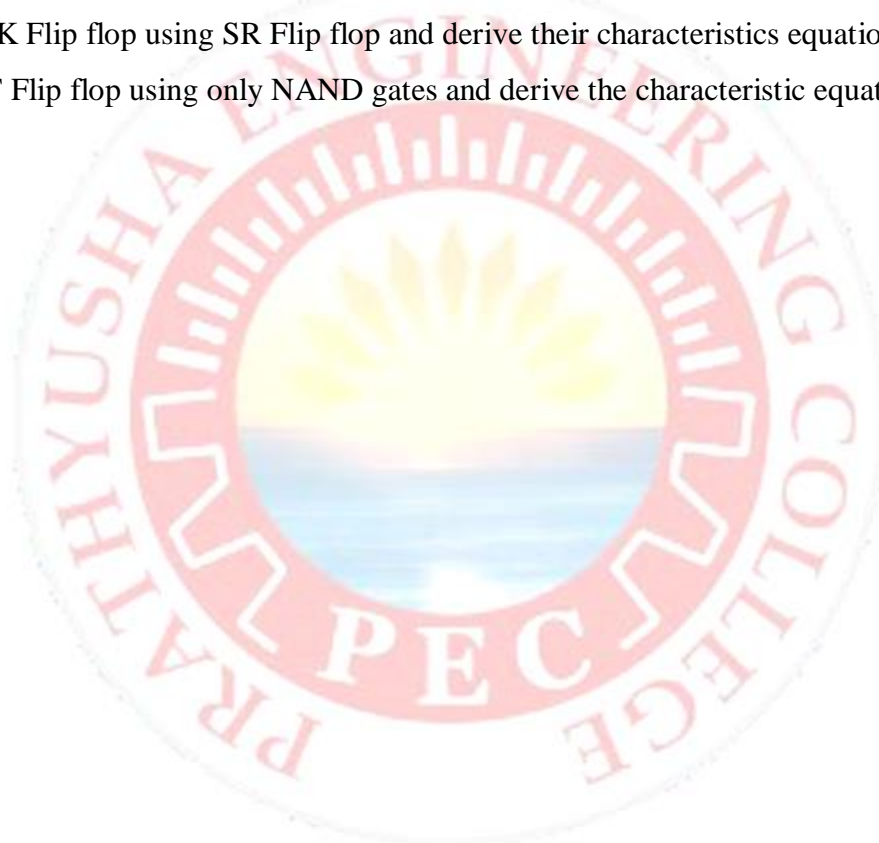
UNIT IV   ASYNCHRONOUS SEQUENTIAL CIRCUITS

PART-A

1. What are the steps for the analysis of asynchronous sequential circuit?

2. What is hazard and give its types?

3. Define ASM chart .List its three basic elements.

4. Define asynchronous sequential circuit.

5. What is a fundamental mode asynchronous sequential circuit?

6. What is a pulse mode asynchronous sequential circuit?

7. Distinguish the classification of sequential circuits and define them.

8. What is a critical race? Why should it be avoided?

9. Define cycle.

10. How can the hazards in combinational circuit be removed?

11. Define race, critical race and non-critical race.

12. Define a primitive flow table.

13. Define a stable state.

14. Define static Hazard.

15. Define Glitch

16. What is a dynamic hazard?

17. What is essential hazard?

18. What is merging?

19. Define compatible?

20. Define maximal compatible.

21. Define closed covering.

22. How does an essential hazard occur?

23. What are the steps for the design of asynchronous sequential circuit?

24. Write short note on shared row state assignment.

25. Write short note on one hot state assignment.

26. What are the problems involved in asynchronous circuits?

PART-B

1. An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are as follows

$$Y_1 = X_1X_2 + X_1Y_2 + X_2Y_1$$

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$$Y_2 = X_2 + X_1Y_1Y_2 + X_1Y_1$$

$$Z = X_2 + Y_1$$

2. Explain the different methods of Race free state assignment.

3. Design a sequential circuit using D flip flop whose state table is specified below

Present state	Next state		Output	
Q0 Q1	X=0	X=1	X=0	X=1
0 0	00	01	0	0
0 1	00	10	0	0
1 0	11	10	0	0
1 1	00	01	0	1

4. Summarize the design procedure for asynchronous sequential circuits.

5. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input x is transferred to Z. When Y is 0, the output does not change for any change in X.

6. What is hazard and list its types? Give the hazard free realization for the Boolean function $f(A,B,C,D) = m(0,2,6,7,8,10,12)$

7. Design the sequential circuit specified by the following state diagram using T flip-flops.
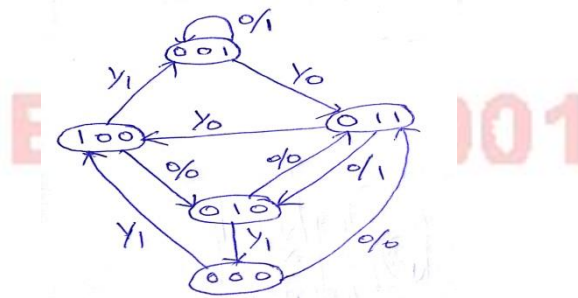
8. Explain in detail about pulse mode and fundamental mode circuits.

9. Design an asynchronous sequential circuit with two inputs x1 and x2 and one output Z.

10. Explain the problems in asynchronous sequential circuits.

11. Explain ASM chart with an example.

UNIT-V   MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS

PART-A

1. What is Volatile and Non-Volatile memory?

2. What is a FPGA?

3. Y=AB'+A'. Implement using ROM.

4. Design XOR gate using ROM.

5. Write the type of semiconductor memories.

6. What is meant by 'static' and 'dynamic' memories?

7. How is individual location in a EEPROM programmed or erased?

8. What is an EAROM?

9. Name any two random access memories.

10. How is the design of combinational and sequential logic circuits possible with PLA?

11. What is RAM?

12. What is ROM?

13. What is PROM?

14. What is EPROM?

15. What is Electrically Erasable PROM (EEPROM)?

16. What is Flash memory?

17. What is PLD?

18. What is PAL?

19. What is PLA?

20. Differentiate ROM & PLD's.

21. What is programmable logic array? How it differs from ROM?

22. What is mask – programmable ROM?

23. Define Cache memory.

24. What are the advantages of RAM?

25. Comparison between PROM, PAL, PLA

26. Draw the CMOS inverter circuit.

27. Define noise margin.

28. What is tri-state logic?

29. Define power dissipation and propagation delay.

30. Define Fan-in & Fan-out.

31. Why totem pole outputs cannot be connected together.

32. State advantages and disadvantages of TTL

PART-B

1. Explain in detail about the working of bipolar SRAM cell and single transistor DRAM cell with neat sketches.
2. Discuss in detail about various types of ROM.
3. Using eight 64 x 8 ROM chips with an enable input and a decoder, design a 512 x 8 ROM.
4. Select a 4096X8 bit ROM memory to store the driver program of the robotic design. The memory chip has two chip select inputs and operates from a 5V power supply. How many pins are needed for the integrated circuit package? Draw a block diagram and label all input and output terminal in ROM.
5. Use PLA with 3 inputs, 4 AND terms and two outputs to implement the following Boolean functions

   $F1(A,B,C)= \sum m(3,5,6,7)$

   $F2(A,B,C)= \sum m(1,2,3,4)$

6. Discuss in detail about the FPGA with suitable diagrams.
7. Design full adder using PAL.
8. Design 16K X 8 RAM using 4K X 8 RAM IC's.
9. Design BCD to excess-3 code converter using the following PLD's.

   i)PROM.

   ii)PLA

   iii) PAL

10. Explain in detail about memory operation with the help of memory cycle timing waveform
11. Explain in detail about the programmable logic devices.
12. Explain in detail about semiconductor memories.
13. Explain in detail about the operation of CMOS NOR gate.
14.Explain the operation of TTL with neat diagram.
15. Explain the characteristics of CMOS logic family.