A Course Material on

LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

By

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EE8451 LINEAR INTEGRATED CIRCUITS AND APPLICATIONS LTPC 3003

OBJECTIVES:

To study the IC fabrication procedure.

To study characteristics; realize circuits; design for signal analysis using Op-amp ICs. To study the applications of Op-amp.

To study internal functional blocks and the applications of special ICs like Timers, PLL circuits, regulator Circuits, ADCs.

UNIT I IC FABRICATION 9

IC classification, fundamental of monolithic IC technology, epitaxial growth, masking and etching,
diffusion of impurities. Realisation of monolithic ICs and packaging. Fabrication of diodes, capacitance, resistance and FETs.

UNIT II CHARACTERISTICS OF OPAMP 9

Ideal OP-AMP characteristics, DC characteristics, AC characteristics,, differential amplifier; frequency
response of OP-AMP; Basic applications of op-amp – Inverting and Non-inverting Amplifiers-V/I & I/V
converters ,summer, differentiator and integrator.

UNIT III APPLICATIONS OF OPAMP 9

Instrumentation amplifier, Log and Antilog Amplifiers, first and second order active filters, , comparators, multivibrators, waveform generators, clippers, clampers, peak detector, S/H circuit, D/A
converter (R- 2R ladder and weighted resistor types), A/D converters using opamps.

UNIT IV SPECIAL ICs 9

Functional block, characteristics & application circuits with 555 Timer Ic-566 voltage controlled
oscillator Ic; 565-phase lock loop Ic ,Analog multiplier ICs.

UNIT V APPLICATION ICs 9

IC voltage regulators –LM78XX,79XX Fixed voltage regulators - LM317, 723 Variable voltage
regulators, switching regulator- SMPS- LM 380 power amplifier- ICL 8038 function generator IC.

TOTAL : 45 PERIODS

TEXT BOOKS:

1. David A.Bell, ‘Op-amp & Linear ICs’, Oxford, 2013.
2. D.Roy Choudhary, Sheil B.Jani, ‘Linear Integrated Circuits’, II edition, New Age, 2003.
3. Ramakant A.Gayakward, ‘Op-amps and Linear Integrated Circuits’, IV edition, Pearson Education, 2003 / PHI. 2000.

REFERENCES:

1. Fiore,”Opamps & Linear Integrated Circuits Concepts & Applications”,Cengage,2010.
2. Floyd ,Buchla,”Fundamentals of Analog Circuits, Pearson, 2013.
3. Jacob Millman, Christos C.Halkias, ‘Integrated Electronics - Analog and Digital circuits system’,Tata McGraw Hill, 2003

CONTENTS

1.1 IC FABRICATION AND CIRCUIT CONFIGURATION FOR LINEAR ICs

1.1.1 Integrated Circuits

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

1.1.2 .Advantages of integrated circuits:

Miniaturization and hence increased equipment density.
Cost reduction due to batch processing.
Increased system reliability due to the elimination of soldered joints.
Improved functional performance.
Matched devices.
Increased operating speeds.
Reduction in power consumption

1.1.3 Classification:

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip). Based upon above requirement two different IC technology namely Monolithic Technology and Hybrid Technology have been developed. In monolithic IC ,all circuit components ,both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bounds.

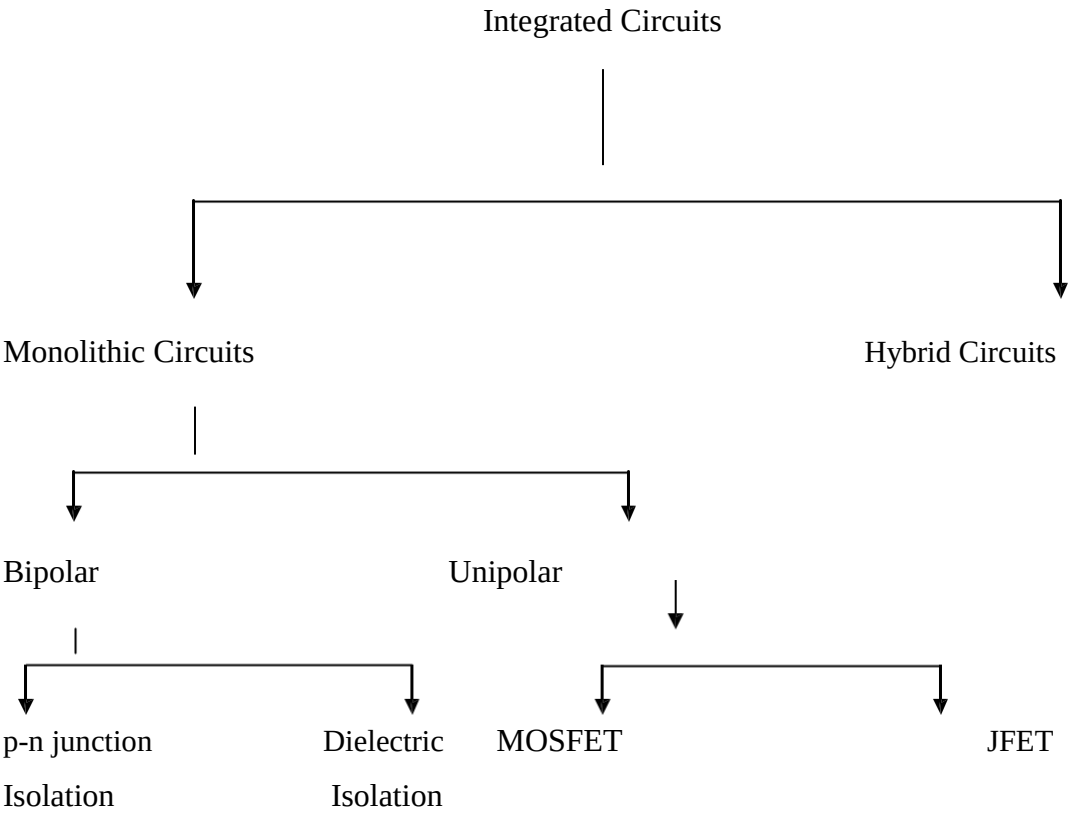
Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimeters. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level

integration. These digital ICs, typically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference

1.2 Classification of ICs:



Generations

1.1.5 SSI, MSI and LSI

The first integrated circuits contained only a few transistors. Called "Small-Scale Integration" (SSI), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors. The term Large Scale Integration was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI. They began to appear in consumer products at the turn of the decade, a typical application being FM inter-carrier sound processing in television receivers.

The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called "Medium-Scale Integration" (MSI). They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

1.1.6 VLSI

The final step in the development process, starting in the 1980s and continuing through the present, was "very large-scale integration" (VLSI). The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2007.

In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors. Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005

1.1.7 ULSI, WSI, SOC and 3D-IC

To reflect further growth of the complexity, the term ULSI that stands for "Ultra-Large Scale Integration" was proposed for chips of complexity of more than 1 million transistors.

Wafer-scale integration (WSI) is a system of building very-large integrated circuits that uses an entire silicon wafer to produce a single "super-chip". Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably

massively parallel supercomputers. The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

System-on-a-Chip (SoC or SOC) is an integrated circuit in which all the components needed for a computer or other system are included on a single chip. The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements.

However, these drawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget: because signals among the components are kept on-die, much less power is require. Three Dimensional Integrated Circuit (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit. Communication between layers uses on-die signaling, so power consumption is much lower than in equivalent separate circuits. Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

1.3 Construction of a Monolithic Bipolar Transistor:

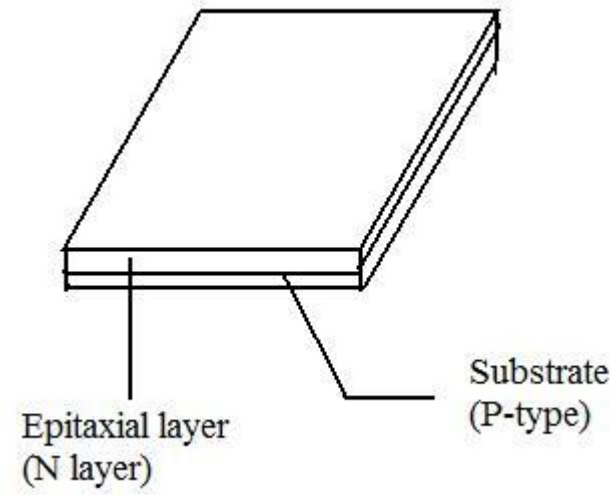
The fabrication of a monolithic transistor includes the following steps.

1. Epitaxial growth
2. Oxidation
3. Photolithography
4. Isolation diffusion
5. Base diffusion
6. Emitter diffusion
7. Contact mask
8. Aluminium metallization
9. Passivation

The letters P and N in the figures refer to type of doping, and a minus (-) or plus (+) with P and N indicates lighter or heavier doping respectively.

1. Epitaxial growth:

The first step in transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current. This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the $V_{CE(Sat)}$ of the device.



The higher collector resistance is reduced by a process called buried layer as shown in figure. In this arrangement, a heavily doped _N' region is sandwiched between the N-type epitaxial layer and P – type substrate. This buried N^+ layer provides a low resistance path in the active collector

region to the collector contact C. In effect, the buried layer provides a low resistance shunt path for the flow of current.

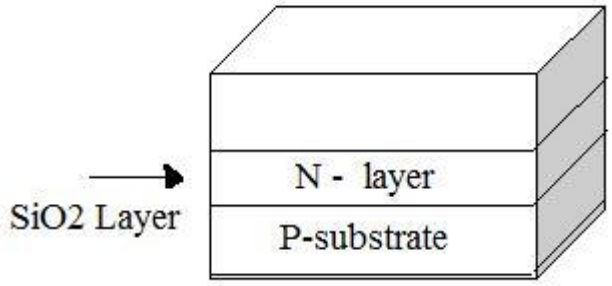
For fabricating an NPN transistor, we begin with a P-type silicon substrate having a resistivity of typically 1Ω-cm, corresponding to an acceptor ion concentration of $1.4 * 10^{15}$ atoms/cm^3 . An oxide mask with the necessary pattern for buried layer diffusion is prepared. This is followed by masking and etching the oxide in the buried layer mask.

The N-type buried layer is now diffused into the substrate. A slow-diffusing material such as arsenic or antimony us used, so that the buried layer will stay-put during subsequent diffusions. The junction depth is typically a few microns, with sheet resistivity of around 20Ω per square.

Then, an epitaxial layer of lightly doped N-silicon is grown on the P-type substrate by placing the wafer in the furnace at 1200^0 C and introducing a gas containing phosphorus (donor impurity). The resulting structure is shown in figure.

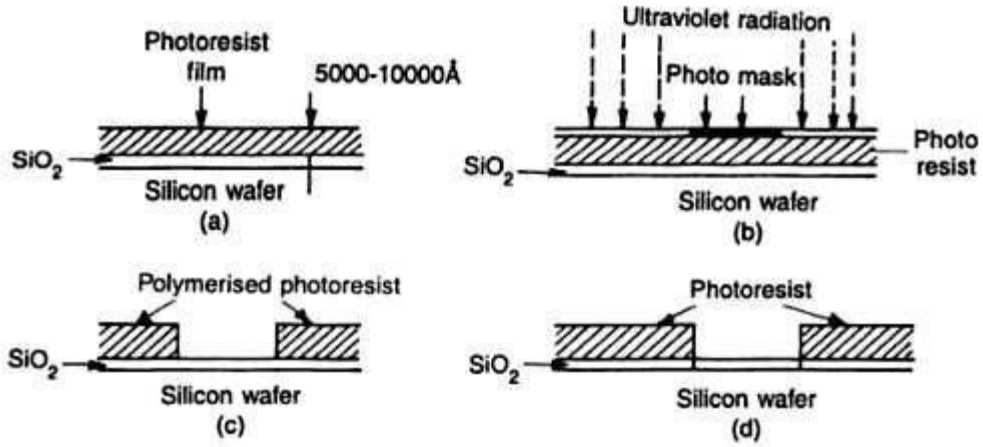
The subsequent diffusions are done in this epitaxial layer. All active and passive components are formed on the thin N-layer epitaxial layer grown over the P-type substrate. Obtaining an epitaxial layer of the proper thickness and doping with high crystal quality is perhaps the most formidable challenge in bipolar device processing.

2. Oxidation:



As shown in figure, a thin layer of silicon dioxide (SiO_2) is grown over the N-type layer by exposing the silicon wafer to an oxygen atmosphere at about 1000^0 C.

3. Photolithography:



The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO_2 layer. As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist). The mask, a black and white negative of the requied pattern, is placed over the structure. When exposed to ultraviolet light, the photo resist under the transparent region of the mask becomes poly-merized. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photoresist film. The polymerized region is cured so that it becomes resistant to corrosion. Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerized photoresist. This creates openings in the SiO_2 layer through which P-type or N-type impurities can be diffused using the isolation diffusion process as shown in figure. After diffusion of impurities, the polymerized photoresist is removed with sulphuric acid and by a mechanical abrasion process.

4. Isolation Diffusion:

The integrated circuit contains many devices. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

The most important techniques for isolation are:

1. PN junction Isolation
2. Dielectric Isolation

In PN junction isolation technique, the P^+ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom. This method generated N-type isolation regions surrounded by P-type moats. If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands.

The individual components are fabricated inside these islands. This method is very economical, and is the most commonly used isolation method for general purpose integrated circuits.

In dielectric isolation method, a layer of solid dielectric such as silicon dioxide or ruby surrounds each component and this dielectric provides isolation. The isolation is both physical and electrical. This method is very expensive due to additional processing steps needed and this is mostly used for fabricating IC‘s required for special application in military and aerospace.

The PN junction isolation diffusion method is shown in figure. The process take place in a furnace using boron source. The diffusion depth must be atleast equal to the epitaxial thickness in order to obtain complete isolation. Poor isolation results in device failures as all transistors might get shorted together. The N-type island shown in figure forms the collector region of the NPN transistor. The heavily doped P-type regions marked P^+ are the isolation regions for the active and passive components that will be formed in the various N-type islands of the epitaxial layer.

5 Base diffusion:

Formation of the base is a critical step in the construction of a bipolar transistor. The base must be aligned, so that, during diffusion, it does not come into contact with either the isolation region or the buried layer. Frequently, the base diffusion step is also used in parallel to fabricate diffused resistors for the circuit. The value of these resistors depends on the diffusion conditions and the width of the opening made during etching. The base width influences the transistor parameters very strongly. Therefore, the base junction depth and resistivity must be tightly controlled. The base sheet resistivity should be fairly high (200- 500Ω per square) so that the base does not inject carriers into the emitter. For NPN transistor, the base is diffused in a furnace using a boron source. The diffusion process is done in two steps, pre deposition of dopants at 900^0 C and driving them in at about 1200^0 C. The drive-in is done in an oxidizing ambience, so that oxide is grown over the base region for subsequent fabrication steps. Figure shows that P-type base region of the transistor diffused in the N-type island (collector region) using photolithography and isolation diffusion processes.

6. Emitter Diffusion:

Emitter Diffusion is the final step in the fabrication of the transistor. The emitter opening must lie wholly within the base. Emitter masking not only opens windows for the emitter, but also for the contact point, which provides a low resistivity ohmic contact path for the emitter terminal.

The emitter diffusion is normally a heavy N-type diffusion, producing low-resistivity layer that can inject charge easily into the base. A Phosphorus source is commonly used so that the diffusion time id shortened and the previous layers do not diffuse further. The emitter is diffused into the base, so that the emitter junction depth very closely approaches the base junction depth. The active base is then a P-region between these two junctions which can be made very narrow by adjusting the emitter diffusion time. Various diffusion and drive in cycles can be used to fabricate the emitter. The Resistivity of the emitter is usually not too critical.

The N-type emitter region of the transistor diffused into the P-type base region is shown below. However, this is not needed to fabricate a resistor where the resistivity of the P-type base region itself will serve the purpose. In this way, an NPN transistor and a resistor are fabricated simultaneously.

7. Contact Mask:

After the fabrication of emitter, windows are etched into the N-type regions where contacts are to be made for collector and emitter terminals. Heavily concentrated phosphorus N^+ dopant is diffused into these regions simultaneously.

The reasons for the use of heavy N^+ diffusion is explained as follows: Aluminium, being a good conductor used for interconnection, is a P-type of impurity when used with silicon. Therefore, it can produce an unwanted diode or rectifying contact with the lightly doped N-material. Introducing a high concentration of N^+ dopant caused the Si lattice at the surface semi-metallic. Thus the N^+ layer makes a very good ohmic contact with the Aluminium layer. This is done by the oxidation, photolithography and isolation diffusion processes.

8. Metallization:

The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices. Aluminium is deposited over the entire wafer by vacuum deposition. The thickness for single layer metal is 1μ m. Metallization is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads as shown in figure.

Metallization is done for making interconnection between the various components fabricated in an IC and providing bonding pads around the circumference of the IC chip for later connection of wires

.

9. Passivation/ Assembly and Packaging:

Metallization is followed by passivation, in which an insulating and protective layer is deposited over the whole device. This protects it against mechanical and chemical damage during subsequent processing steps. Doped or undoped silicon oxide or silicon nitride, or some combination of them, are usually chosen for passivation of layers. The layer is deposited by chemical vapour deposition (CVD) technique at a temperature low enough not to harm the metallization.

1.4 Transistor Fabrication:

PNP Transistor:

The integrated PNP transistors are fabricated in one of the following three structures.

1. Substrate or Vertical PNP
2. Lateral or horizontal PNP and
3. Triple diffused PNP

Substrate or Vertical PNP:

The P-substrate of the IC is used as the collector, the N-epitaxial layer is used as the base and the next P-diffusion is used as the emitter region of the PNP transistor. The structure of a vertical monolithic PNP transistor Q_1 is shown in figure. The base region of an NPN transistor structure is formed in parallel with the emitter region of the PNP transistor.

The method of fabrication has the disadvantage of having its collector held at a fixed negative potential. This is due to the fact that the P-substrate of the IC is always held at a negative potential normally for providing good isolation between the circuit components and the substrate.

Triple diffused PNP:

This type of PNP transistor is formed by including an additional diffusion process over the standard NPN transistor processing steps. This is called a triple diffusion process, because it involves an additional diffusion of P-region in the second N-diffusion region of a NPN transistor. The structure of the triple diffused monolithic PNP transistor Q_2 is also shown in the below figure.

This has the limitations of requiring additional fabrication steps and sophisticated fabrication assemblies.

1.1.10 Lateral or Horizontal PNP:

This is the most commonly used form of integrated PNP transistor fabrication method. This has the advantage that it can be fabricated simultaneously with the processing steps of an NPN transistor and therefore it requires as the base of the PNP transistor. During the P-type base diffusion process of NPN transistor, two parallel P-regions are formed which make the emitter and collector regions of the horizontal PNP transistor.

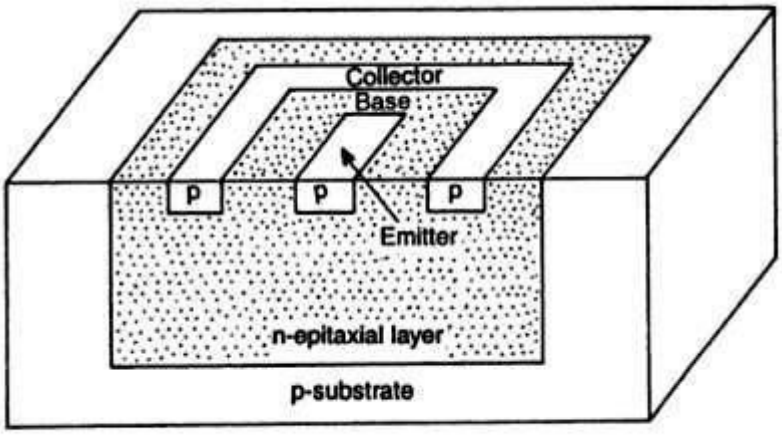


Fig. 1.17 A *pnp* lateral transistor

Comparison of monolithic NPN and PNP transistor:

Normally, the NPN transistor is preferred in monolithic circuits due to the following reasons:

1. The vertical PNP transistor must have his collector held at a fixed negative voltage.

2. The lateral PNP transistor has very wide base region and has the limitation due to the lateral diffusion of P-type impurities into the N-type base region. This makes the photographic mask making, alignment and etching processes very difficult. This reduces the current gain of lateral PNP transistors as low as 1.5 to 30 as against 50 to 300 for a monolithic NPN transistor.

3. The collector region is formed prior to the formation of base and emitter diffusion. During the later diffusion steps, the collector impurities diffuse on either side of the defined collector junction. Since the N-type impurities have smaller diffusion constant compared to P-type impurities the N-

type collector performs better than the P-type collector. This makes the NPN transistor preferable for monolithic fabrication due to the easier process control.

Transistor with multiple emitters: The applications such as transistor- transistor logic (TTL) require multiple emitters. The below figure shows the circuit sectional view of three N-emitter regions diffused in three places inside the P-type base. This arrangement saves the chip area and enhances the component density of the IC.

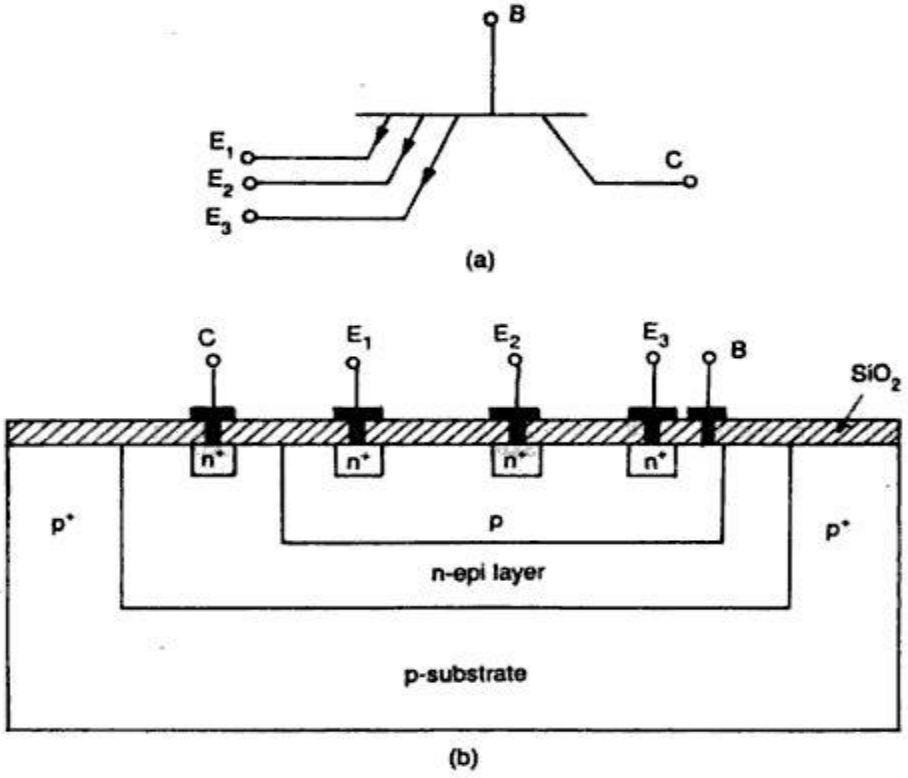


Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

1.5 Schottky Barrier Diode:

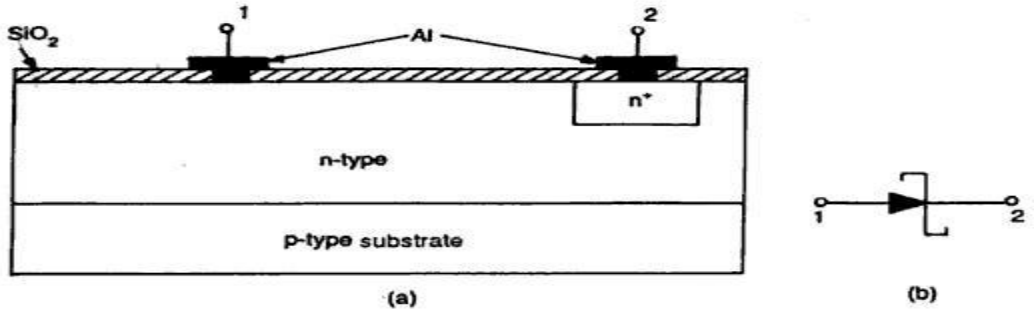


Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

The metal contacts are required to be ohmic and no PN junctions to be formed between the metal and silicon layers. The N^+ diffusion region serves the purpose of generating ohmic contacts. On the other hand, if aluminium is deposited directly on the N-type silicon, then a metal semiconductor diode can be said to be formed. Such a metal semiconductor diode junction exhibits the same type of V-I Characteristics as that of an ordinary PN junction.

The cross sectional view and symbol of a Schottky barrier diode as shown in figure. Contact 1 shown in figure is a Schottky barrier and the contact 2 is an ohmic contact. The contact potential between the semiconductor and the metal generated a barrier for the flow of conducting electrons from semiconductor to metal. When the junction is forward biased this barrier is lowered and the electron flow is allowed from semiconductor to metal, where the electrons are in large quantities.

The minority carriers carry the conduction current in the Schottky diode whereas in the PN junction diode, minority carriers carry the conduction current and it incurs an appreciable time delay from ON state to OFF state. This is due to the fact that the minority carriers stored in the junction have to be totally removed. This characteristic puts the Schottky barrier diode at an advantage since it exhibits negligible time to flow the electron from N-type silicon into aluminum almost right at the contact surface, where they mix with the free electrons. The other advantage of this diode is that it has less forward voltage (approximately 0.4V). Thus it can be used for clamping and detection in high frequency applications and microwave integrated circuits.

1.1.12 Schottky transistor:

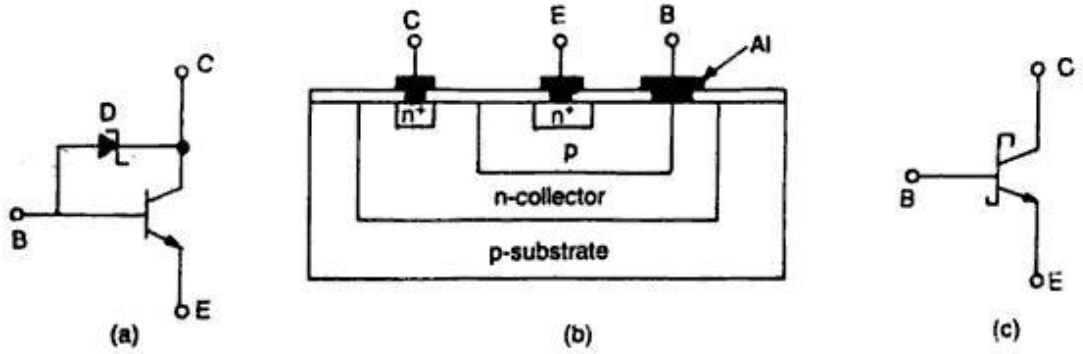


Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

The cross-sectional view of a transistor employing a Schottky barrier diode clamped between its base and collector regions is shown in figure. The equivalent circuit and the symbolic representation of the Schottky transistor are shown in figure. The Schottky diode is formed by allowing aluminium metallization for the base lead which makes contact with the N-type collector region also as shown in figure.

When the base current is increased to saturate the transistor, the voltage at the collector C reduces and this makes the diode Ds conduct. The base to collector voltage reduces to 0.4V, which is less the cut-in-voltage of a silicon base-collector junction. Therefore, the transistor does not get saturated.

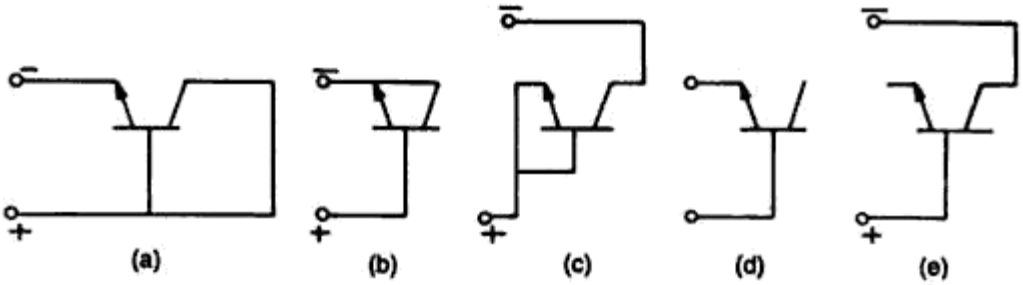
1.6 Monolithic diodes:

The diode used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector –base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

Characteristic	(a) $V_{CB} = 0$	(b) $V_{CE} = 0$	(c) $V_{EB} = 0$	(d) $I_C = 0$	(e) $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95



1.1.14 Integrated Resistors:

A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are 1. Diffused 2. epitaxial 3. Pinched and 4. Thin film techniques.

1.1.15 Diffused Resistor:

The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The N-type emitter diffusion and P-type base diffusion are commonly used to realize the monolithic resistor.

The diffused resistor has a severe limitation in that, only small valued resistors can be fabricated. The surface geometry such as the length, width and the diffused impurity profile determine the resistance value. The commonly used parameter for defining this resistance is called the sheet resistance. It is defined as the resistance in ohms/square offered by the diffused area.

In the monolithic resistor, the resistance value is expressed by

$R = R_s$ 1/w where R= resistance offered (in ohms)

R_s = sheet resistance of the particular fabrication process involved (in ohms/square)

l = length of the diffused area and

w = width of the diffused area.

The sheet resistance of the base and emitter diffusion in 200Ω/Square and 2.2Ω/square respectively. For example, an emitter-diffused strip of 2mil wide and 20 mil long will offer a resistance of 22Ω. For higher values of resistance, the diffusion region can be formed in a zig-zag fashion resulting in larger effective length. The poly silicon layer can also be used for resistor realization.

1.1.16 Epitaxial Resistor:

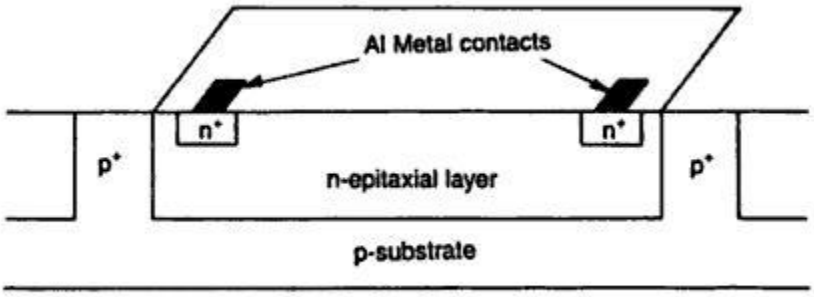


Fig. 1.23 (a) Epitaxial resistor

The N-epitaxial layer can be used for realizing large resistance values. The figure shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two N^+ aluminium metal contacts.

1.1.17 Pinched resistor:

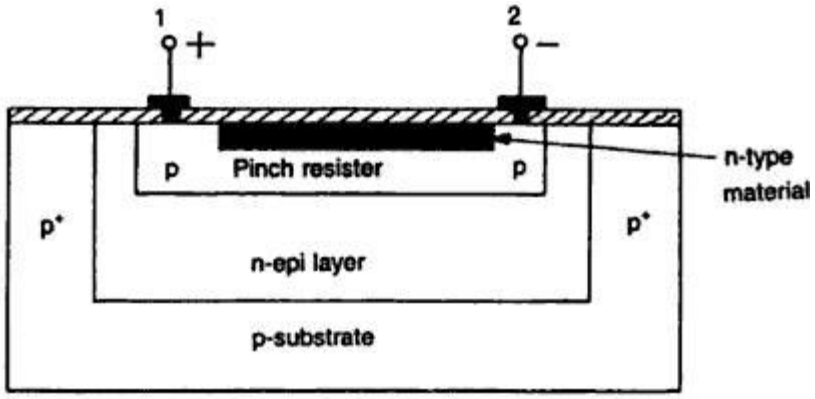


Fig. 1.23 (b) Cross-sectional view of a pinch resistor

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a comparatively smaller area. In the structure shown, no current can flow in the N-type material

since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the width narrows down and hence it acts as a pinched resistor.

1.1.18Thin film resistor:

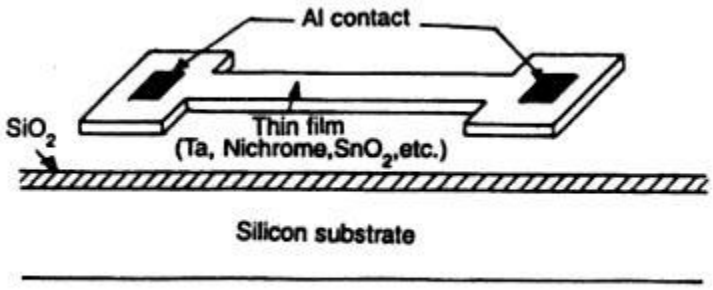


Fig. 1.23 (c) Cross-section of a thin film resistor

The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than 1μm is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome (NiCr) is used for this process. Desired geometry is achieved using masked etching processes to obtain suitable value of resistors. Ohmic contacts are made using aluminium metallization as discussed in earlier sections.

The cross-sectional view of a thin film resistor as shown in figure. Sheet resistances of 40 to 400Ω/ square can be easily obtained in this method and thus 20kΩ to 50kΩ values are very practical.

The advantages of thin film resistors are as follows:

1. They have smaller parasitic components which makes their high frequency behaviour good.
2. The thin film resistor values can be very minutely controlled using laser trimming.
3. They have low temperature coefficient of resistance and this makes them more stable.

The thin film resistor can be obtained by the use of tantalum deposited over silicon dioxide layer. The main disadvantage of thin film resistor is that its fabrication requires additional processing steps.

1.7 Monolithic Capacitors:

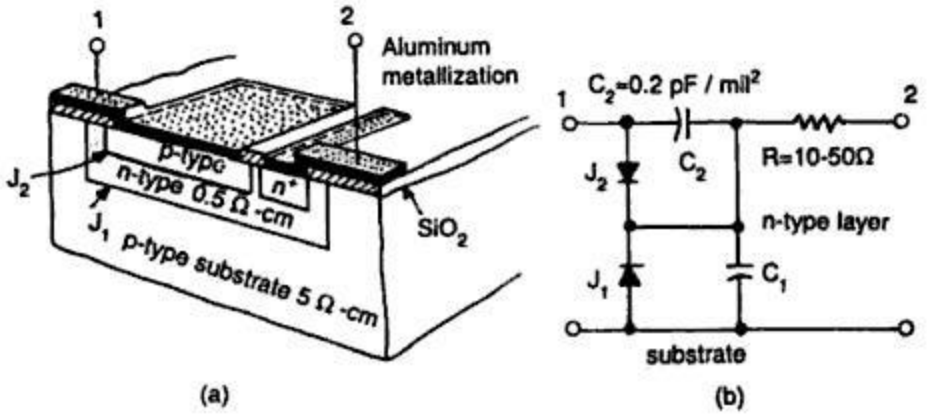


Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor is a reverse biased PN junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

C α A, where a is the area of the junction and

C α T , where t is the thickness of the depletion layer.

The capacitance value thus obtainable can be around 1.2nF/mm^2 .

The thin film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between 0.3 and 0.8nF/mm^2 .

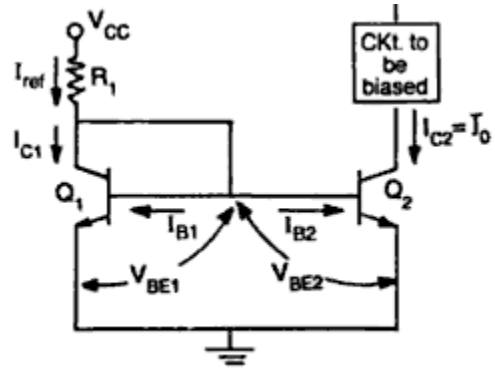
1.1.20 Inductors:

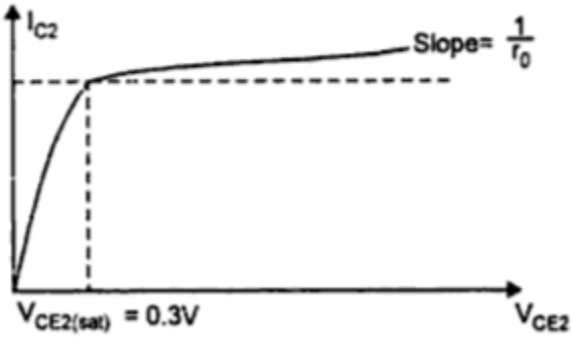
No satisfactory integrated inductors exist. If high Q inductors with inductance of values larger than 5μH are required, they are usually supplied by a wound inductor which is connected externally to the chip. Therefore, the use of inductors is normally avoided when integrated circuits are used.

1.8 CURRENT MIRROR AND CURRENT SOURCES:

Constant current source(Current Mirror):

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in fig 1





Transistors Q_1&Q_2 are matched as the circuit is fabricated using IC technology. Base and emitter of Q_1&Q_2 are tied together and thus have the same V_{BE}. .In addition, transistor Q1 is connected as a diode by shorting it s collector to base. The input current I_{ref} flows through the diode connected transistor Q1 and thus establishes a voltage across Q_1.

This voltage in turn appears between the base and emitter of Q_2 .Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}

As long as Q2 is maintained in the active region ,its collector current $I_{C2}=I_o$ will be approximately equal to I_{ref} .

Since the output current Io is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

Analysis:

The collector current I_{C1} and I_{C2} for the transistor Q1 and Q2 can be approximately expressed as

$$I_{C1} \approx \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad \text{---------(1)}$$

$$I_{C2} \approx \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad \text{----------(2)}$$

From equation (1)&(2)

$$I_{C2} \quad \frac{V_{BE2}}{V_T}$$

$$I_{C1} = e \qquad \text{----------(3)}$$

Since $V_{BE1}=V_{BE2}$ we obtain

$I_{C2}=I_{C1}=I_C=I_O$

Also since both the transistors are identical , $\beta_1 = \beta_2 = \beta$ KCL at the collector of Q_1 gives

$I_{ref}= I_{C1}+I_{B1}+I_{B2}$

$$I_{C1}\left(1+\frac{2}{\beta}\right) \quad \text{----------(4)}$$

$$=I_{C1}+\frac{\beta_1}{\beta_2}I_C$$

solving Eq (4).

I_C may be expressed as

$$I_C = \frac{\beta}{\beta+2} I_{ref} \qquad \text{----------(5)}$$

Where I_{ref} from fig can be seen to be

$$I_{ref} = V_{CC} @ \frac{V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} \text{ (as } V_{BE} \text{=0.7V is small)}$$

From Eq.5 for $\beta >> 1$, $\frac{\beta}{\beta+2}$ is almost unity and the output current I_0 is equal to the reference current, I_{ref} which for a given R_1 is constant. Typically I_o varies by about 3% for $50 \leq \beta \leq 200$.

It is possible to obtain current transfer ratio other than unity simple by controlling the area of the emitter-base junction (EBJ) of the transistor Q_2 . For example, if the area of EBJ of Q_2 is 4 times that of Q1,then

$I_O=4\, I_{ref}$

The output resistance of the current source is the output resistance,r_0 of Q2,

$R_0=I_{02}=\approx= \frac{V_A}{I_{ref}}$ [V_A is the Early voltage]

I_O

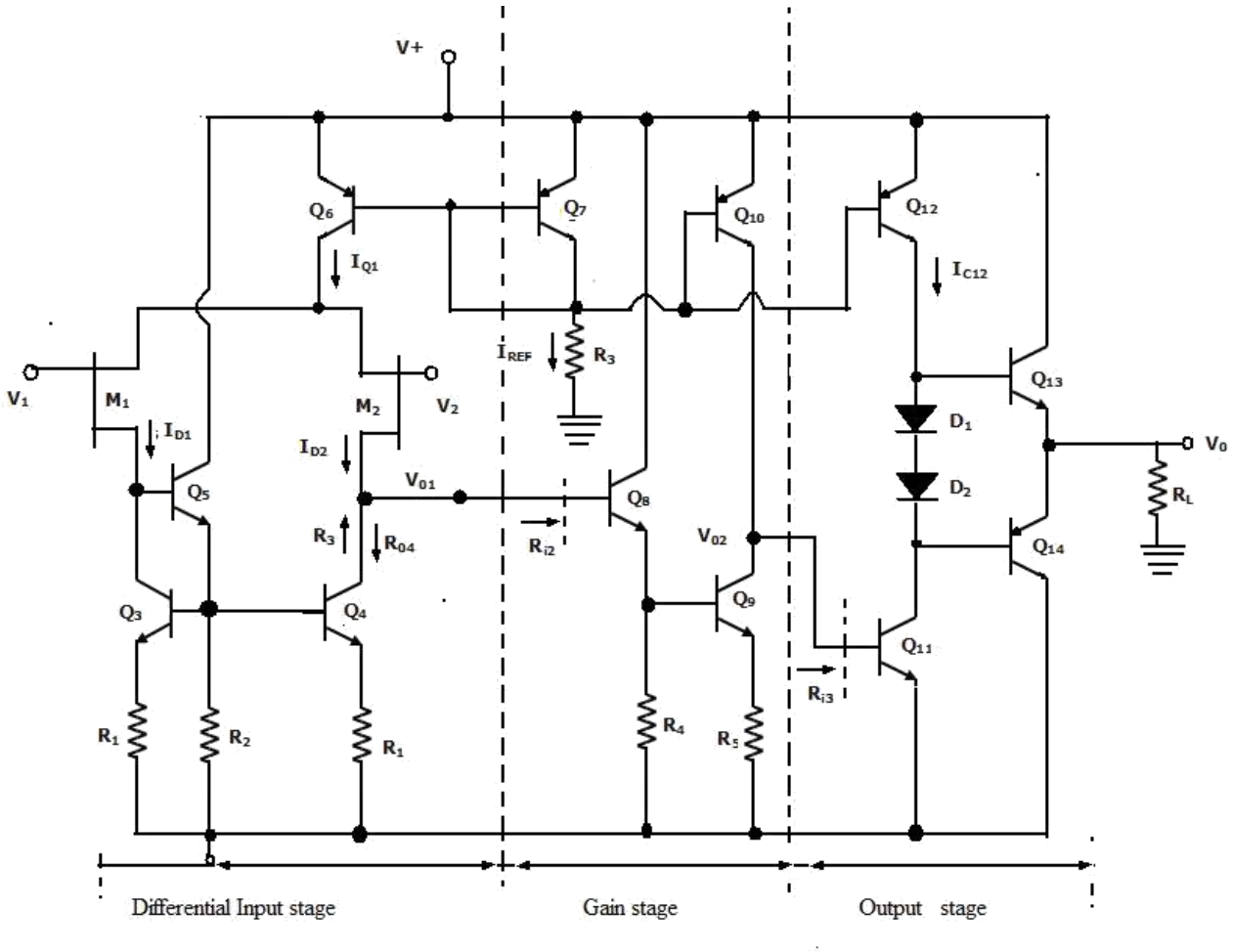
The circuit however operates as a constant current source as long as Q_2 remains in the active region.

UNIT II
Characteristics of op-amp

2.0 General Operational Amplifier:

An operational amplifier generally consists of three stages, anmely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 10^4 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. The figure shows a general op-amp circuit using JFET input devices.



2.1.1 Input stage:

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3 , Q_4 , and Q_5 . the bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the output resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5 . A single ended output is taken out at the collector of Q_4 .

MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input resistance.

Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9 . The V_{BE} drop across Q_9 and drop across R_5 constitute the voltage drop across R_4 , and this voltage sets the current through Q_8 . It can be set to a small value, such that the base current of Q_8 also is very less.

2.1.2 Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and Q_{12}, through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain A_V of the op-amp is the product of voltage gain of each stage as given by $A_V = |A_d | |A_2 ||A_3 |$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

2.1 IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. the input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V, and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current I_{REF} for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R_5. The widlar current source formed by Q_{11} , Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of Q_{10}.

ransistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The reference bias current I_{REF} also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13A} providing bias current for output stage and Q_{13B} providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two V_{BE} drops of potential difference between the bases of Q_{14} and Q_{18} .

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain.

The transistors Q5, Q6 and Q7 along with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q_6. the two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q_3 and Q_4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q_3 and Q_4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20} . Hence, they provide an effective loss output resistance and current gain.

The output of the gain stage is connected at the base of Q_{22} , which is connected as an emitter – follower providing a very high input resistance, and it offers no appreciable loading effect on the

gain stage. It is biased by transistor Q_{13A} which also drives Q_{18} and Q_{19}, that are used for establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.

2.1.4 Ideal op-amp characteristics:

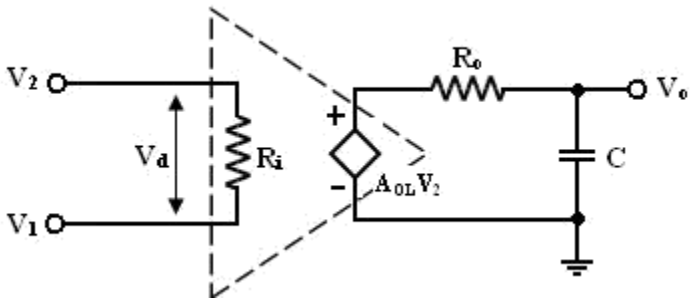
1. Infinite voltage gain A.
2. Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage.
3. Zero output resistance R_o, so that the output can drive an infinite number of other devices.
4. Zero output voltage, when input voltage is zero.
5. Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.
6. Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
7. Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

2.2 AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.

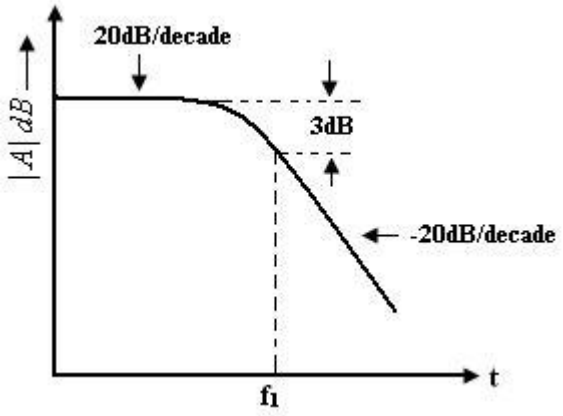


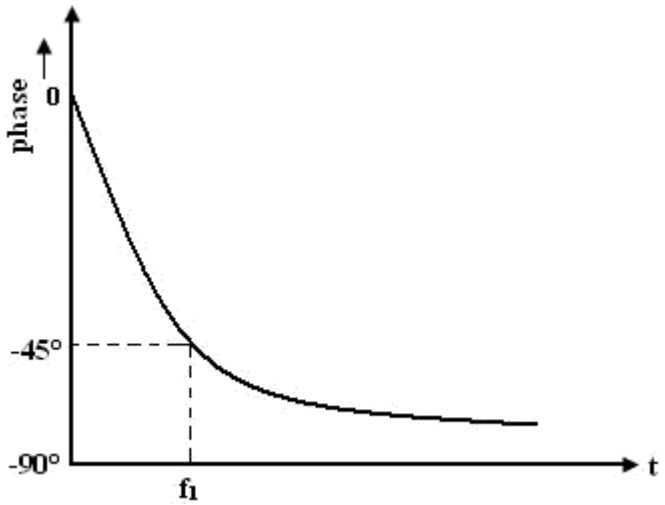
There is one pole due to R_0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig.

f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as,

The magnitude and phase angle characteristics from eqn (29) and (30)

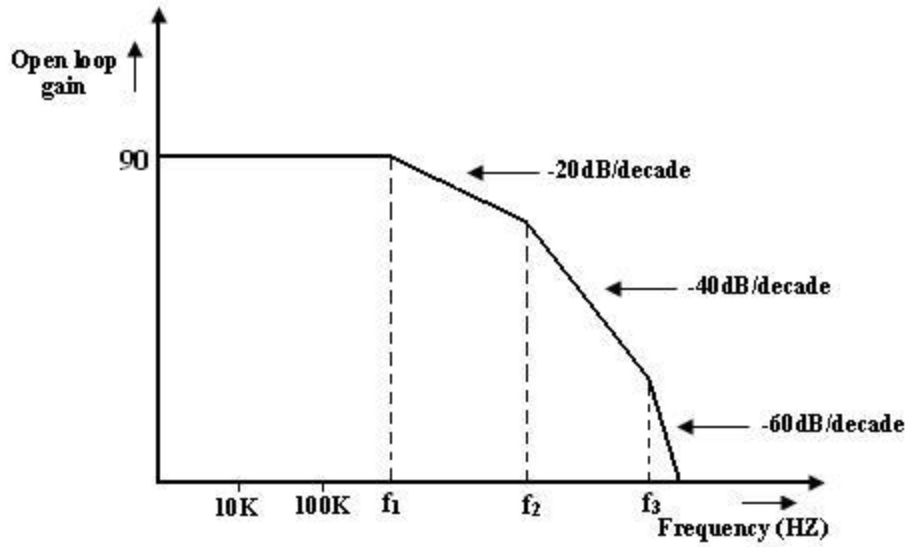
1. For frequency $f << f_1$ the magnitude of the gain is 20 log A_{OL} in dB.
2. At frequency $f = f_1$ the gain in 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.
3. For $f >> f_1$ the fain roll-off at the rate off -20dB/decade or -6dB/decade.





From the phase characteristics that the phase angle is zero at frequency f =0.

At the corner frequency f_1 the phase angle is -45^0 (lagging and a infinite frequency the phase angle is -90^0 . It shows that a maximum of 90^0 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency.

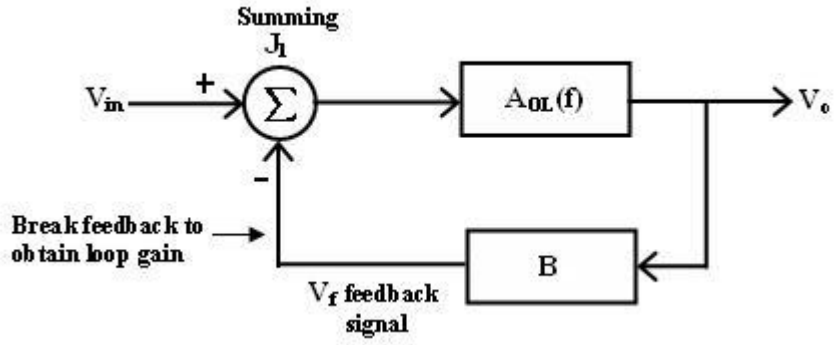


2.1.6 Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The

criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.



The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred ―Transfer frequency' From fig we represented it by A_{OL} (f) which is given by

A_{OL} (f) = V_0 /Vin if V_f = 0. -----(1)

where A_{OL} (f) = open loop volt gain. The closed loop gain A_f is given

by $A_F = V_0$ /Vin

$A_F = A_{OL}$ / (1+(A_{OL}) (B) ----(2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method:1:

Determine the phase angle when the magnitude of (A_{OL}) (B) is 0dB (or) 1. If phase angle is > .-180^0 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (A_{OL}) (B) is 0dB (or) 1. If phase angle is > .-180^0 , If the magnitude is –ve decibels then the system is stable. However, the some systems the

phase angle of a system may reach -180^0 , under such conditions method 1 must be used to determine the system stability.

2.3 Slew Rate:

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

2.1.8 Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{--------} \quad (1)$$

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

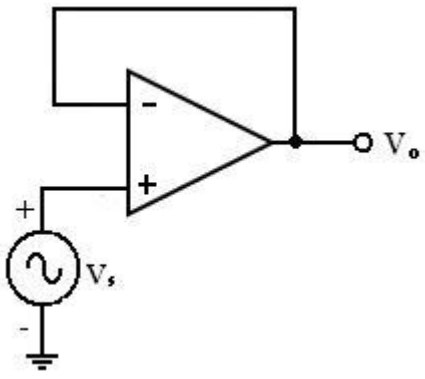
For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is

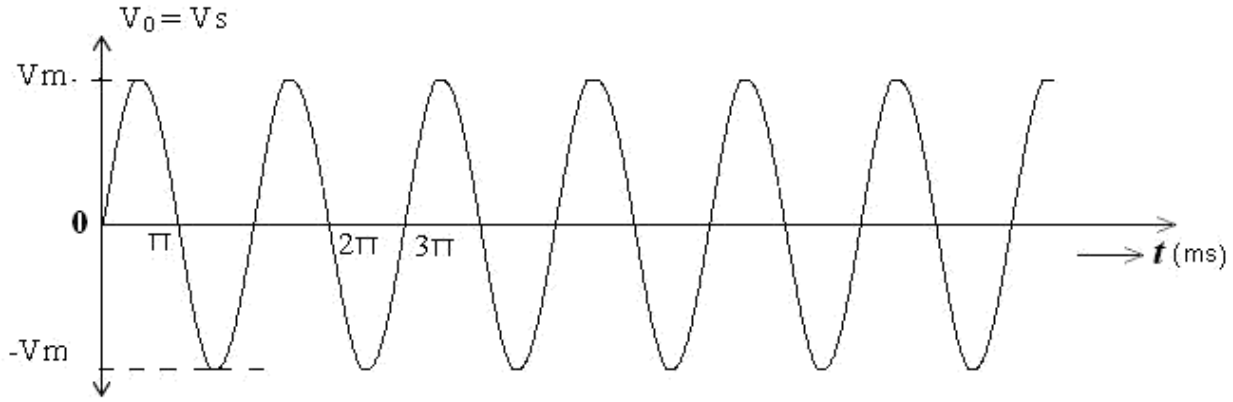
$$SR = dVc/dt\ |max = Imax/C .$$

For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .

If Vs = Vm Sinwt then output V_0 = Vm sinwt . The rate of change of output is given by

$$dV_0/dt = Vm\ w\ coswt.$$





Input and Output Waveforms

The max rate of change of output across when coswt =1

(i.e) SR = $dV_0/dt|_{max} = wVm$.

SR = $2\pi fVm$ V/s = $2\pi fVm$ v/ms.

Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by

fmax (Hz) = Slew rate/6.28 * Vm .

called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

2.4 DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

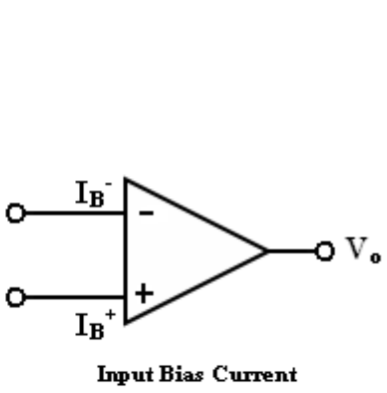
1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

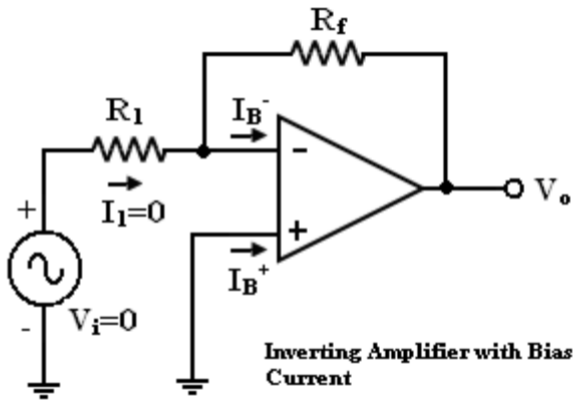
2.1.10 Input bias current:

The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

- In an ideal op-amp, we assumed that no current is drawn from the input terminals.
- The base currents entering into the inverting and non-inverting terminals (I_B^- & I_B^+ respectively).

- Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs.
- Manufacturers specify the input bias current I_B





So, $I_B = \frac{I_B^- + I_B^+}{2}$

If input voltage V_i = 0V. The output Voltage V_o should also be (V_o = 0)

I_B = 500nA

We find that the output voltage is offset by,

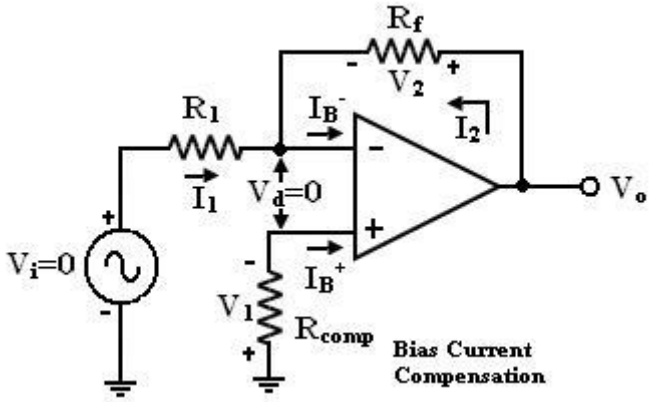
$$V_o = I_B R_f$$

Op-amp with a 1M feedback resistor

V_o = 5000nA X 1M = 500mV

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated. Where a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.



Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$-V_1+0+V_2-V_o = 0$ (or)

$V_o = V_2 - V_1$ ——>(3)

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived a

$V_1 = I_B^+ R_{comp}$ (or)

$I_B^+ = V_1/R_{comp}$ ——>(4)

The node =a‘ is at voltage ($-V_1$). Because the voltage at the non-inverting input terminal is ($-V_1$). So with $V_i = 0$ we get,

$I_1 = V_1/R_1$ ——>(5)

$I_2 = V_2/R_f$ ——>(6)

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$I_2 = V_1/R_f$ ——>(7)

KCL at node =a‘ gives,

$I_B^- = I_2 + I_1$

$$I_B = \quad R_f \quad R_1 \qquad +$$

Assume $I_B^- = I_B^+$ and using equation (4) & (8) we get

$$R^{comp} = R_1 + R_f$$

$R_{comp} = R_1 \parallel R_f$ ———>(9)

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

2.1.11 Input offset current:

- Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.
- Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$|I_{os}| = I_B^+ - I_B^-$ ——>(10)

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$V_1 = I_B^+ R_{comp}$ ——>(11)

And $I_1 = V_1/R_1$ ——>(12)

KCL at node =a‘ gives,

Again

$V_0 = I_2 R_f - V_1$

$V_o = I_2 R_f - I_B^+ R_{comp}$

$V_o = 1M\ \Omega \times 200nA$

$V_o = 200mV$ with $V_i = 0$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R_1 must be kept large.
- R_1 large, the feedback resistor R_f must also be high. So as to obtain reasonable gain.

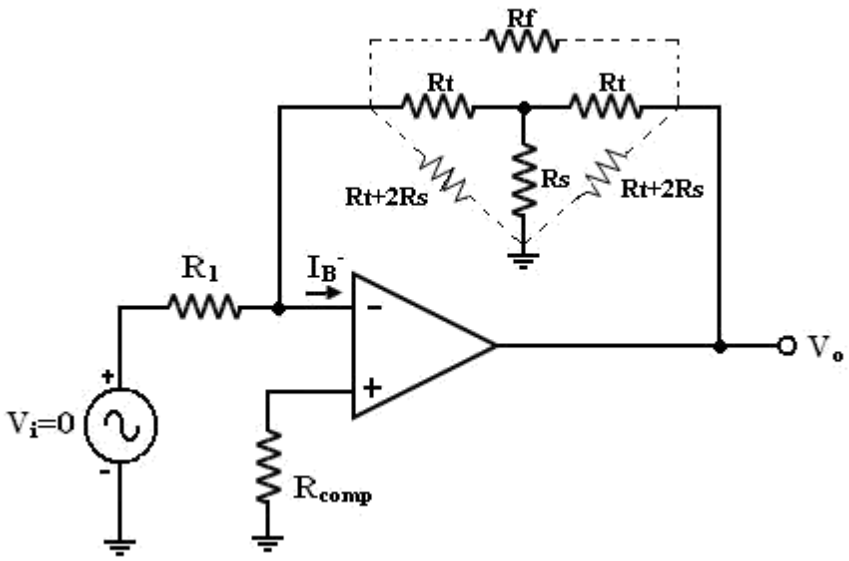
The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

- The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

To design T- network first pick $R_t << R_f/2$ ——>(18)

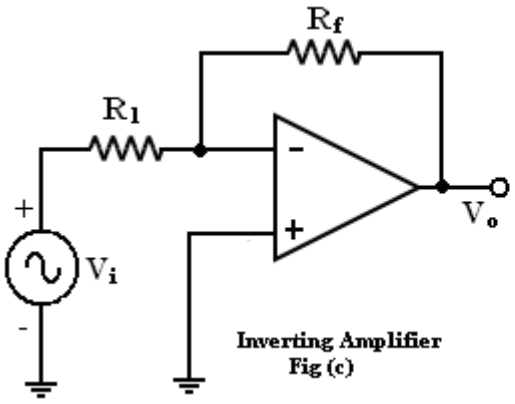
Then calculate $R_s = R_f 2 R_t$



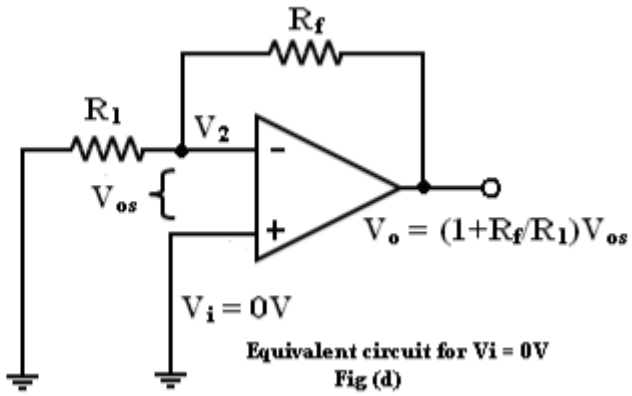
2.1.12 Input offset voltage:

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [$V_o \neq 0$ with $V_i = 0$]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (V_o) = 0.

This voltage is called input offset voltage V_{os}. This is the voltage required to be applied at the input for making output voltage to zero ($V_o = 0$).



Inverting Amplifier
Fig (c)



Equivalent circuit for Vi = 0V
Fig (d)

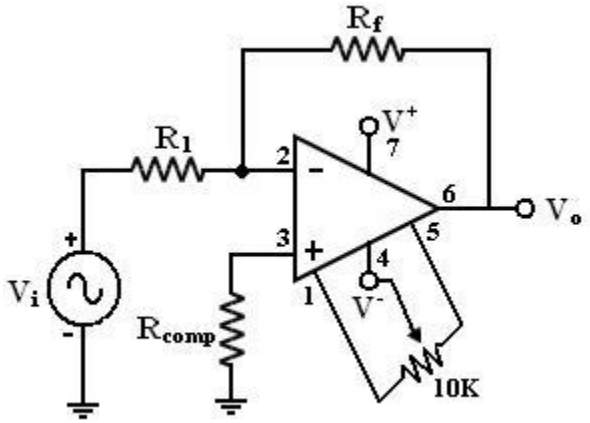
Let us determine the V_{os} on the output of inverting and non-inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

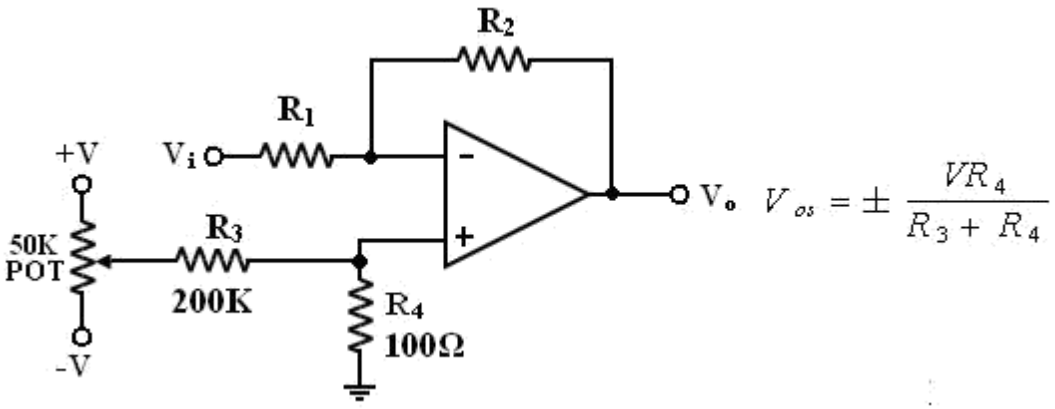
The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone(V_{os}).

This is because I_B and V_{os} could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op-amp provide offset compensation pins to nullify the offset voltage.

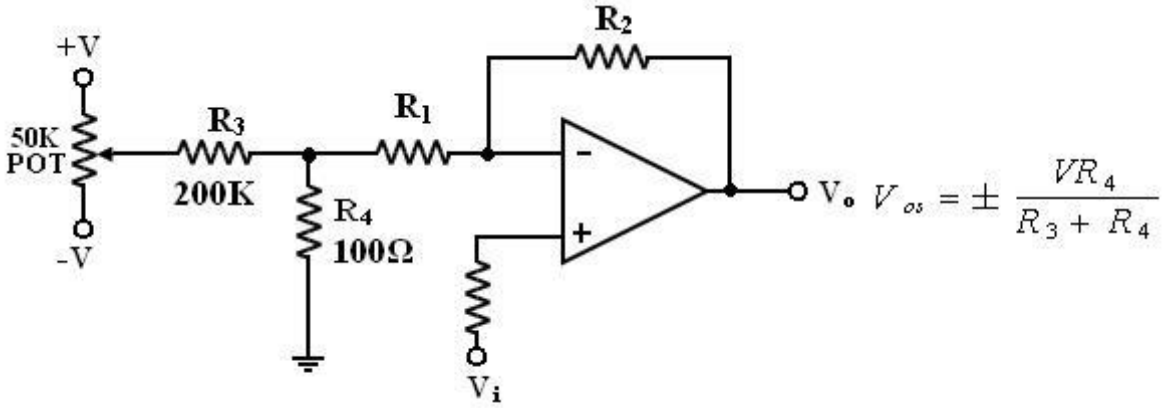
- 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4.
- The position of the wipes is adjusted to nullify the offset voltage.



When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.



2.5 Non-inverting amplifier:



Thermal drift:

- Bias current, offset current, and offset voltage change with temperature.
- A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift.
- Offset current drift is expressed in nA/ºC.
- These indicate the change in offset for each degree Celsius change in temperature.

2.1.14 Openloop-op-amp Configuration:

The term open-loop indicates that no feedback in any form is fed to the input from the output. When connected in open – loop, the op-amp functions as a very high gain amplifier. There are three open – loop configurations of op-amp namely,

1. differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

The above classification is made based on the number of inputs used and the terminal to which the input is applied. The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltage.

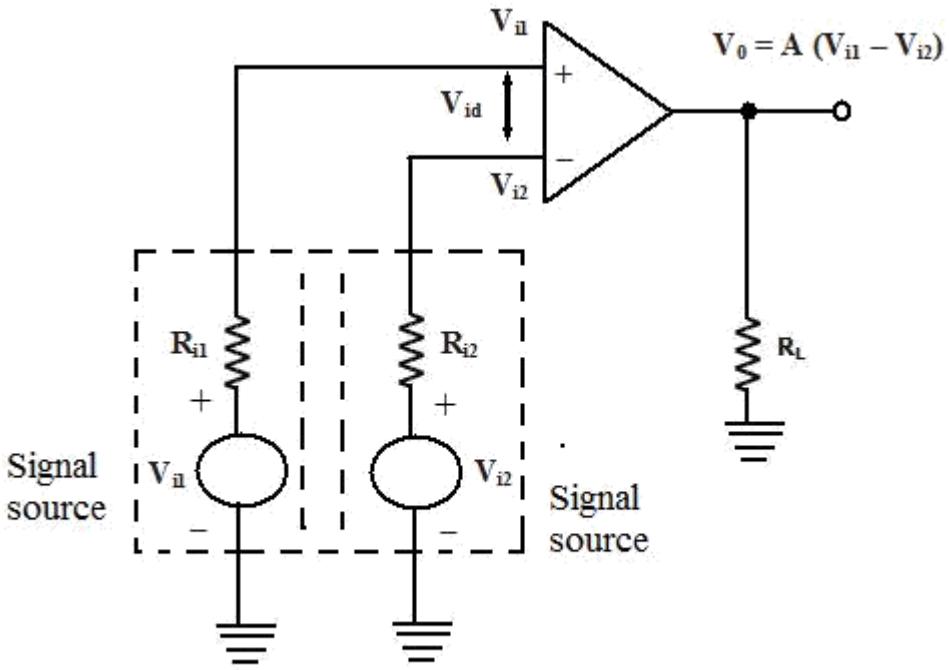
2.1.15 Open–loop Differential Amplifier:

In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages. Figure shows the open-loop differential amplifier configuration.

The input voltages are represented by V_{i1} and V_{i2}. The source resistance R_{i1} and R_{i2} are negligibly small in comparison with the very high input resistance offered by the op-amp, and thus the voltage drop across these source resistances is assumed to be zero. The output voltage V_0 is given by

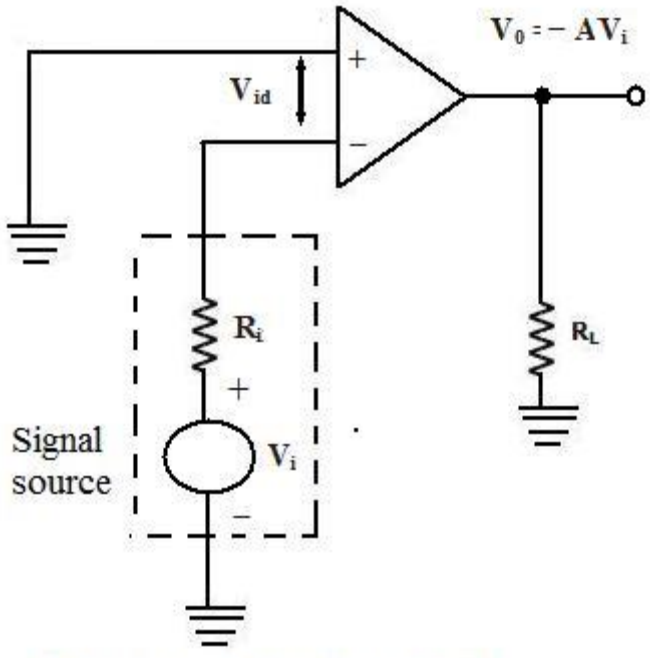
$V_0 = A(V_{i1} - V_{i2})$

where A is the large signal voltage gain. Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages. This is the reason why this configuration is called a differential amplifier. In open – loop configurations, the large signal voltage gain A is also called open-loop gain A.



Open - loop Differential Amplifier

2.6 Inverting amplifier:



Open - loop Inverting Amplifier

In this configuration the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground. Figure shows the circuit of an open – loop inverting amplifier.

The output voltage is 180^0 out of phase with respect to the input and hence, the output voltage V_0 is given by,

$V_0 = -AV_i$

Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and in phase – shifted by 180^0.

2.1.17 Non-inverting Amplifier:

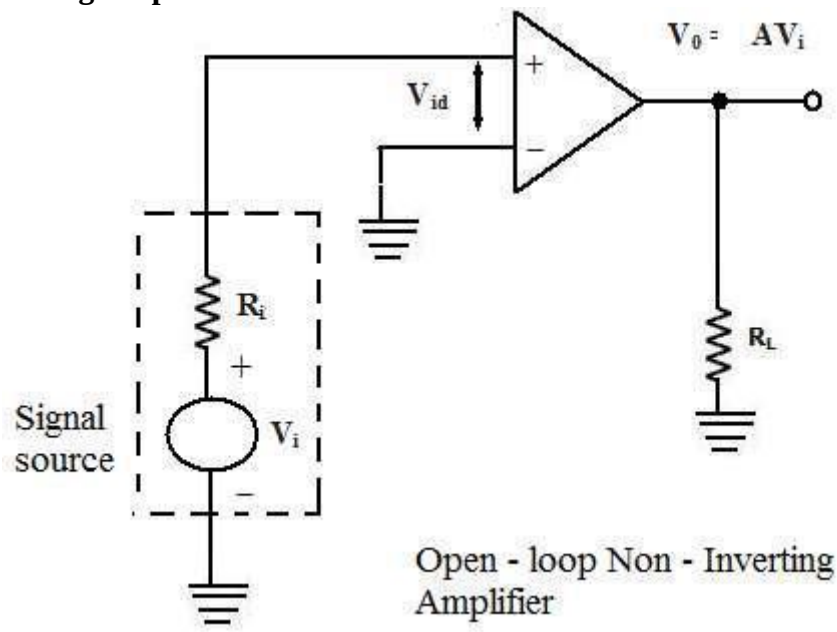


Figure shows the open – loop non- inverting amplifier. The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.

The input signal is amplified by the open – loop gain A and the output is in-phase with input signal.

$V_0 = AV_i$

In all the above open-loop configurations, only very small values of input voltages can be applied. Even for voltages levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp shown in figure. Thus, when operated in the open-loop configuration, the output of the op-amp is either in negative or positive saturation, or switches between positive and negative saturation levels. This prevents the use of open – loop configuration of op-amps in linear applications.

2.2.1 Limitations of Open – loop Op – amp configuration:

Firstly, in the open – loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open – loop gain of the op-amp. This feature actually makes it possible to amplify very low frequency signal of the order of microvolt or even less, and the amplification can be achieved accurately without any distortion. However, signals of such magnitudes are susceptible to noise and the amplification for those application is almost impossible to obtain in the laboratory.

Secondly, the open – loop gain of the op – amp is not a constant and it varies with changing temperature and variations in power supply. Also, the bandwidth of most of the open- loop op amps is negligibly small. This makes the open – loop configuration of op-amp unsuitable for ac applications. The open – loop bandwidth of the widely used 741 IC is approximately 5Hz. But in almost all ac applications, the bandwidth requirement is much larger than this.

For the reason stated, the open – loop op-amp is generally not used in linear applications. However, the open – loop op amp configurations find use in certain non – linear applications such as comparators, square wave generators and astable multivibrators.

2.2.2 Closed – loop op-amp configuration:

The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out- of-phase by 180^0 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback. Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback.

An op – amp that uses feedback is called a closed – loop amplifier. The most commonly used closed – loop amplifier configurations are 1. Inverting amplifier (Voltage shunt amplifier) 2. Non-Inverting amplifier (Voltage – series Amplifier)

2.2.3 Inverting Amplifier:

The inverting amplifier is shown in figure and its alternate circuit arrangement is shown in figure, with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op – amp through resistor R_1 .

The op – amp has an open – loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 180^0 out – of – phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is negative or degenerative.

3.1 Differential amplifier:

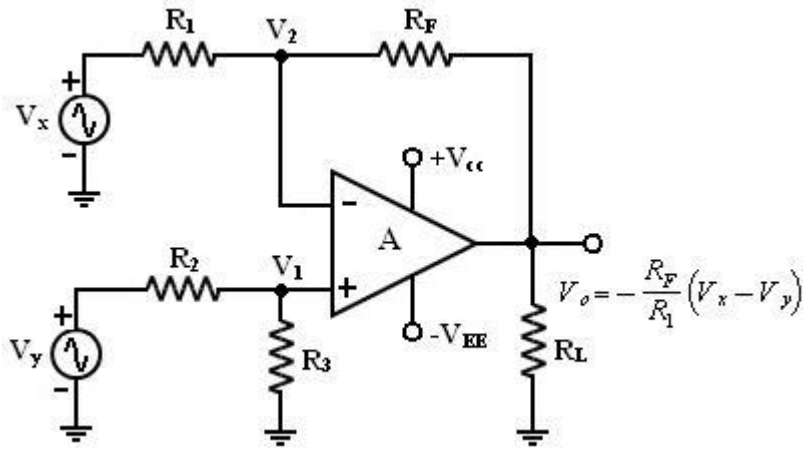
We will evaluate 2 different arrangements of the differential amplifier with -ve feedback. Classify these arrangements according to the number of op-amps used. i.e

1. Differential amplifier with one op-amp
2. Differential amplifier with two op-amps.

Differential amplifier are used in instrumentation and industrial applications to amplify differences between 2 input signals such as output of the wheat stone bridge circuit.

Differential amplifier preferred to these application because they are better able to reject common mode (noise) voltages than single input circuit such as inverting and non-inverting amplifier.

2.2.5 Differential Amplifier with one op-amp:



To analyse this circuit by deriving voltage gain and input resistance. This circuit is a combination of inverting and non-inverting amplifier. (i.e) When V_x is reduced to zero the circuit is non-inverting amplifier and when V_y is reduced to zero the circuit is inverting amplifier.

2.2.6 Voltage Gain:

The circuit has 2 inputs V_x and V_y . Use superposition theorem, when V_y = 0V, becomes inverting amplifier. Hence the o/p due to V_x only is

Similarly, when V_x = 0V, becomes Non-inverting amplifier having a voltage divider network composed of R_2 and R_3 at the Non – inverting input.

Note : the gain of the differential amplifier is same as that of inverting amplifier.

2.2.7 Input Resistance:

The input resistance R_{if} of the differential amplifier is resistance determined looking into either one of the 2 input terminals with the other grounded,

With V_y = 0V,

Inverting amplifier, the input resistance which is,

$R_{iFx} \approx R_1$ ----------

(26.a) Similarly, ,V_x = 0V,

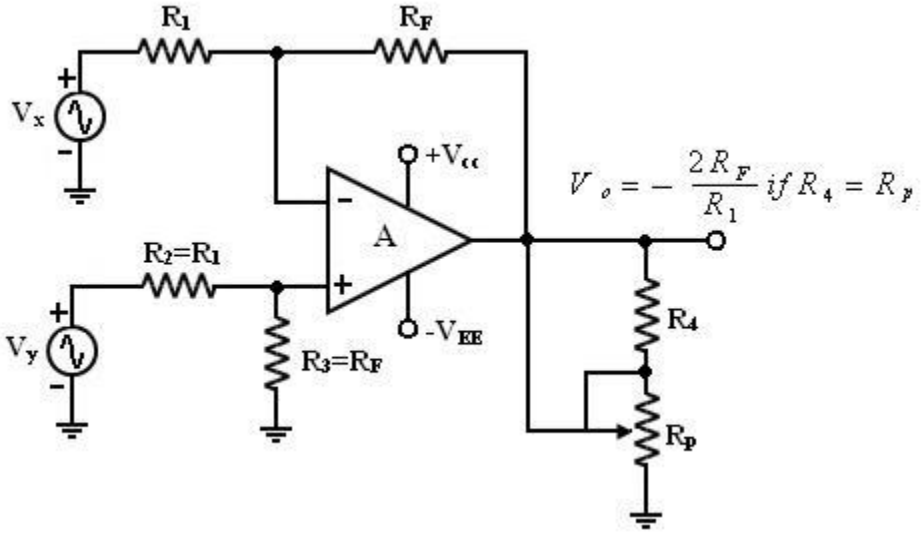
Non-inverting amplifier, the input resistance which is,

$R_{iFy} \approx (R_2 + R_3)$ ------(26.b)

V_x and V_y are not the same. Both the input resistance can be made equal, if we modify the basic differential amplifier. Both R_1 and $(R_2 + R_3)$ can be made much larger than the source resistances. So that the loading of the signal sources does not occur.

Note: If we need a variable gain, we can use the differential amplifier. In this circuit $R_1 = R_2$, $R_F = R_3$ and the potentiometer $R_p = R_4$.

Depending on the position of the wiper in R voltage can be varied from the closed loop gain of -$2R_F/R_1$ to the open loop gain of A.



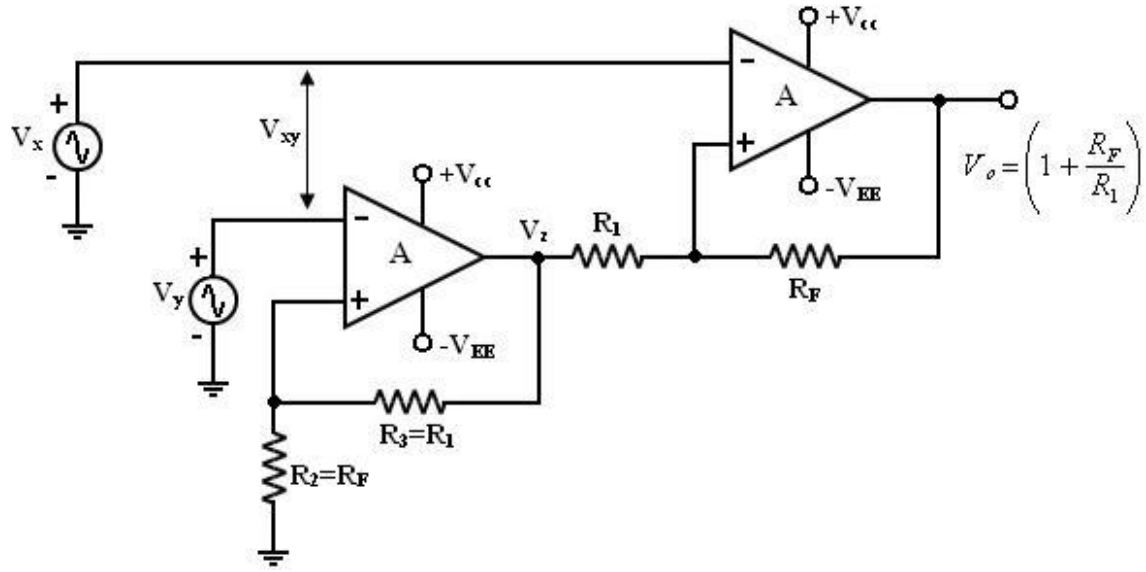
2.2.8. Differential Amplifier with 2 op-amps:

We can increase the gain of the differential amplifier and also increase the input resistance R_{if} if we use 2 op-amps.

2.2.9 Voltage gain:

It is compares of 2 stages 1. Non-inverting

. Differential amplifier with gain.



By finding the gain of these 2 stages, we can obtain the overall gain of the circuit,

2.2.10 Input Resistance:

The input resistance Rif of the differential amplifier is the resistance determined from either one of the two non-inverting terminals with the other grounded. The first stage A_1 is the non-inverting amplifier, its input resistance is

$R_{iFy} = R_i (1+AB)$ -----(29. a)

Where Ri = open loop input resistance of the op-amp.

$B=R_2/R_2+R_3$

Similarly, with V_y shorted to ground ($V_y = 0$ V), the 2nd stage (A_2) also becomes non-inverting amplifier, whose input resistance is

$R_{iFx} = R_i (1+AB)$ -----(29. b)

Where Ri = open loop input resistance of the op-

amp $B = R_1 /(R_1 + R_F)$

Since $R_1 = R_3$ and $R_F = R_2$, the Rify ≠ RiFx because the loading of the input sources V_x and V_y may occur. (Or)

The output signal may be smaller in amplitude than expected. This possible reduction in the amplitude of the output signal is drawback of differential amplifier. To overcome this:

With proper selection of components, both RiFy and RiFx can be made much larger than the sources resistance so that the loading of the input sources does not occur.

2.2.11 Output resistance and Bandwidth of differential amplifier with feedback:

The output resistance of the differential amplifier should be the same as that of the non-inverting amplifier expect that $B = 1/A_D$ (i.e)

$R_{OF} = R_0 /(1+A/A_D)$ ----- (30)

A_D = closed loop gain of the differential amplifier

R_0 = output resistance of the op-amp

A = open – loop volt gain of the op-amp

Remember that A_D is different for differential amplifier.In the case of Inverting and Non-inverting amplifier, the bandwidth of the differential amplifier also depends on the closed loop gain of the amplifier and is given by,

f_F = Unity gain Bandwidth closed loop gain A_D (or) $f_F = (A) (f_0)$

UNIT III

3.1 APPLICATION OF OP-AMP

The basic inverting amplifier configuration using an op-amp with input impedance Z_1 and feedback impedance Z_f .

If the impedance Z_1 and Z_f are equal in magnitude and phase, then the closed loop voltage gain is -1,and the input signal will undergo a 180^0 phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign.

Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier

Referring the above diagram, if the ratio $Z_f / Z_1 = k$, a real constant, then the closed loop gain is –k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output. Usually, in such applications, Z_f and Z_1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

3.1.2 PHASE SHIFT CIRCUITS

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

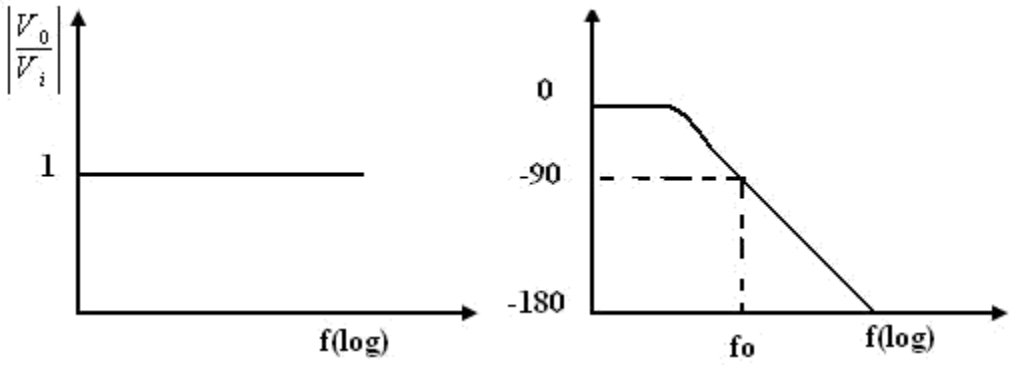
This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

3.1.3 Phase-lag circuit:

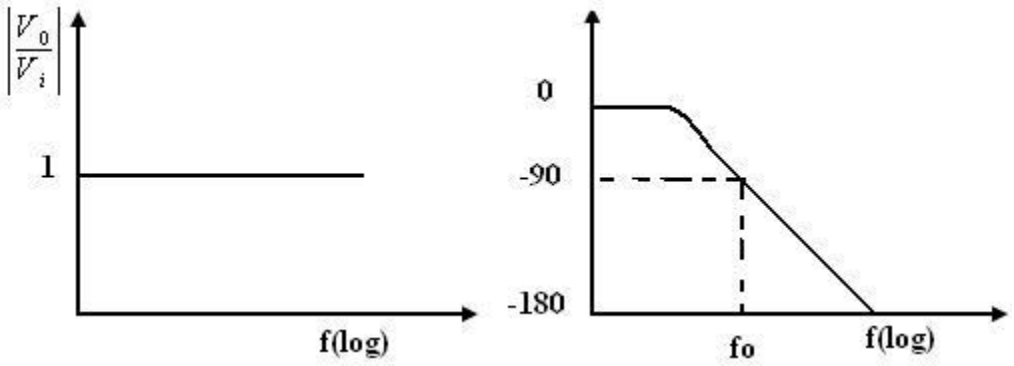
Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit

.



The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their



3.2 Voltage follower:

If $R_1=\infty$ and Rf=0 in the non inverting amplifier configuration .

The amplifier act as a unity-gain amplifier or voltage follower.

That is

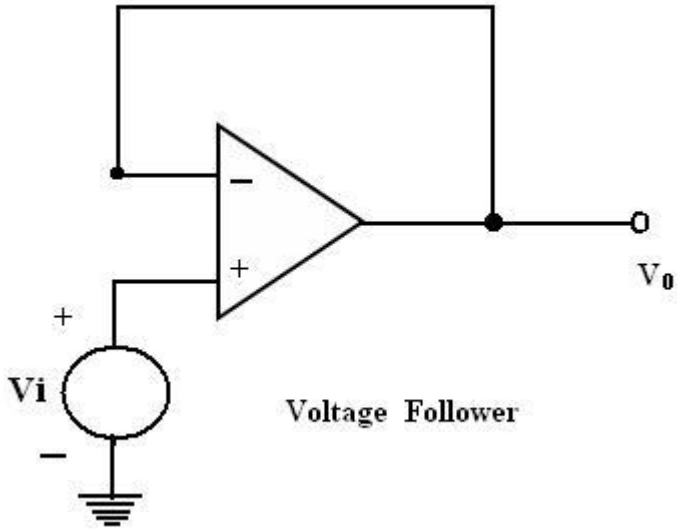
$$_vA = 1 + \frac{R^f}{R}$$

Since $\frac{R_f}{R_1} = 1$

The circuit consist of an op-amp and a wire connecting the output voltage to the input ,i.e the output voltage is equal to the input voltage, both in magnitude and phase.$V_0=V_i$

Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of MΩ and very low output impedance.

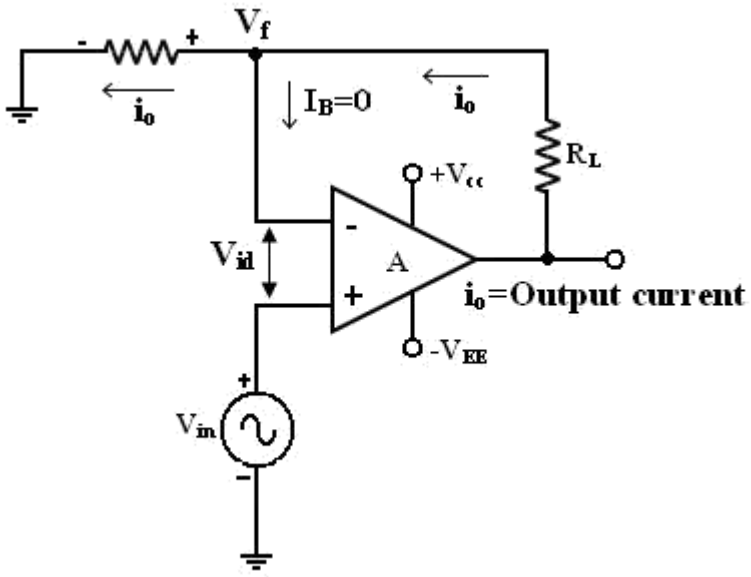
Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.



Voltage Follower

3.1.5 Voltage to Current Converter with floating loads (V/I):

1. Voltage to current converter in which load resistor R_L is floating (not connected to ground).
2. Vin is applied to the non inverting input terminal, and the feedback voltage across R_1 devices the inverting input terminal.
3. This circuit is also called as a current – series negative feedback amplifier.
4. Because the feedback voltage across R_1 (applied Non-inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id} .



Writing KVL for the input loop,

$$Vin = V_{id} + V_f$$

V_{id} t 0v , *since A is very large* A

$$Vin = V_f$$

$$Vin = R_1 \, i_0 \quad \text{` or a}$$

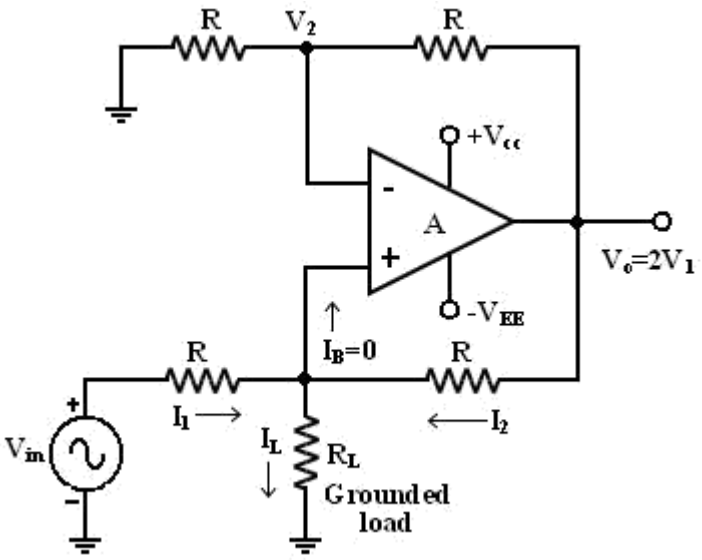
From the fig input voltage Vin is converted into output current of Vin/R_1 [Vin -> i_0] . In other words, input volt appears across R_1. If R_1 is a precision resistor, the output current (i_0 = Vin/R_1) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED
4. Zener diode testers.

3.1.6 Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.



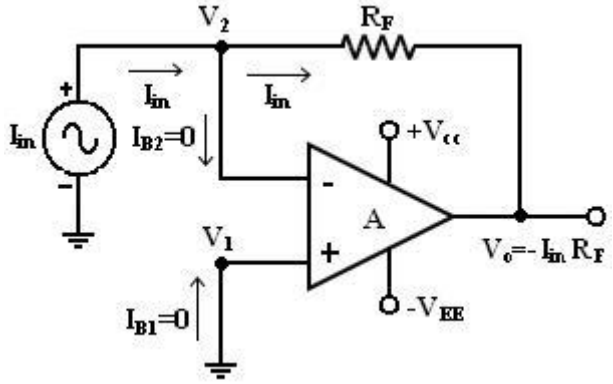
Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V_1 at the non-inverting (+) terminals and
2. To establish relationship between V_1 and the load current I_L

. Applying KCL at node V_1 we can write that,

3.3 Current to Voltage Converter (I –V):



1. Open – loop gain a of the op-amp is very large. $V_1 \approx V_2$ @@@@ `1a
2. Input impedance of the op-amp is very high. (i.e) the currents entering into the 2 input

terminals is very small. I_B [1]

$$= I_{B_2}$$

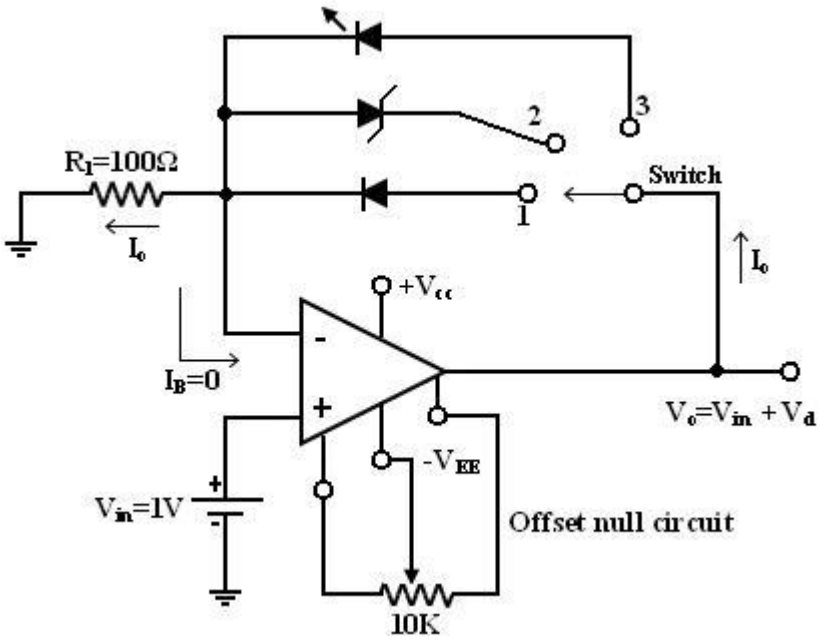
$= 0$ ---(2)

3.1.8 Sensitivity of the I – V converter:

1. The output voltage $V_0 = -R_F I_{in}$.
2. Hence the gain of this converter is equal to $-R_F$. The magnitude of the gain (i.e) is also called as sensitivity of I to V converter.
3. The amount of change in output volt ΔV_0 for a given change in the input current ΔI_{in} is decide by the sensitivity of I-V converter.
4. By keeping R_F variable, it is possible to vary the sensitivity as per the requirements.

3.1.9 Applications of V-I converter with Floating Load:

1. Diode Match finder:



In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing R_L with a diode. When the switch is in position 1: (Diode Match Finder) Rectifierr diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R_1 . For Vin = 1V and $R_1 = 100\Omega$, the current through this

$I_0 = Vin/R_1 = 1/100 = 10mA.$

As long as V_0 and R_1 constant, I_0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage. The output voltage is equal to (Vin + V_D) V_0

= Vin + V_D . To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Zener diode Tester:

(When the switch position 2)

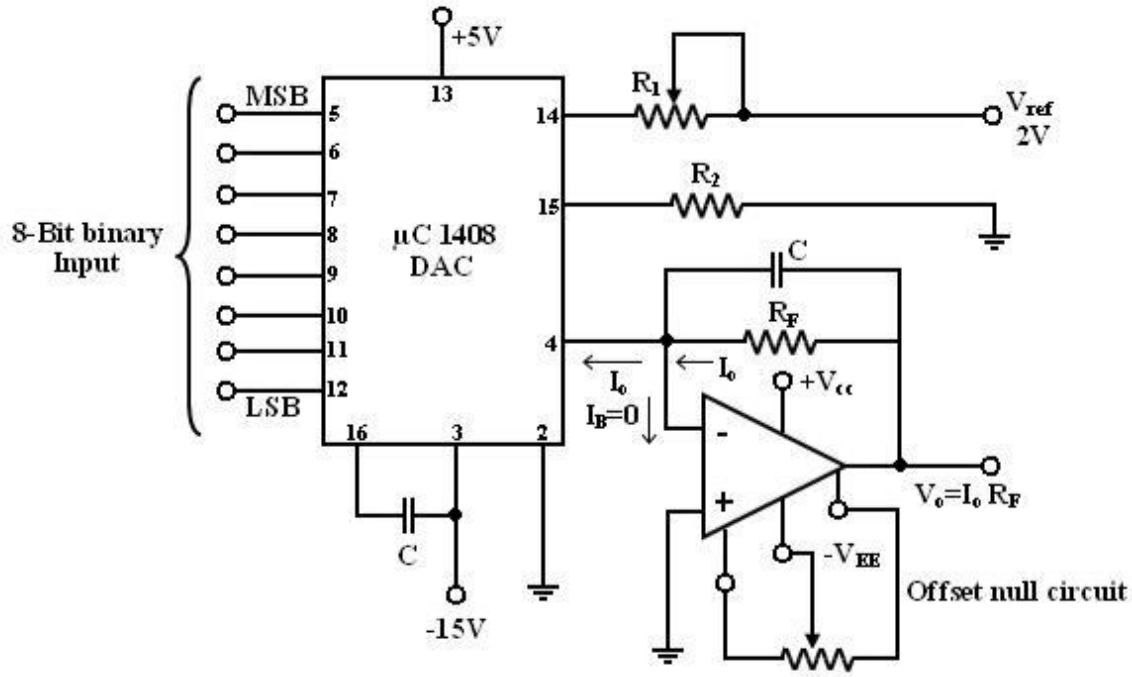
when the switch is in position 2, the circuit becomes a zener diode tester. The circuit can be used to find the breakdown voltage of zener diodes. The zener current is set at a constant value by Vin and R_1. If this current is larger than the knee current (I_{ZK}) of the zener, the zenerr blocks (V_z) volts. For Ex:

I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1v , R_1 = 100Ω Since the current through the zener is , I_0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R_1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

3.1.10 Applications of I – V Converter:



One of the most common use of the current to voltage converter is

1. Digital to analog Converter (DAC)
2. Sensing current through Photodetector. Such as photocell, photodiodes and photovoltaic cells.

Photoconductive devices produce a current that is proportional to an incident energy or light (i.e) It can be used to detect the light.

3.1.11 DAC using I – V converter:

It shows a combination of a DAC and current to voltage converter. The 8 digit binary signal is the input to the DAC and V_0 is the corresponding analog output of the current to voltage converter. The outputu of the DAC is current I_0, the value of which depends on the logic state (0 or 1), of the binary inputs as indicated by the following eqn.

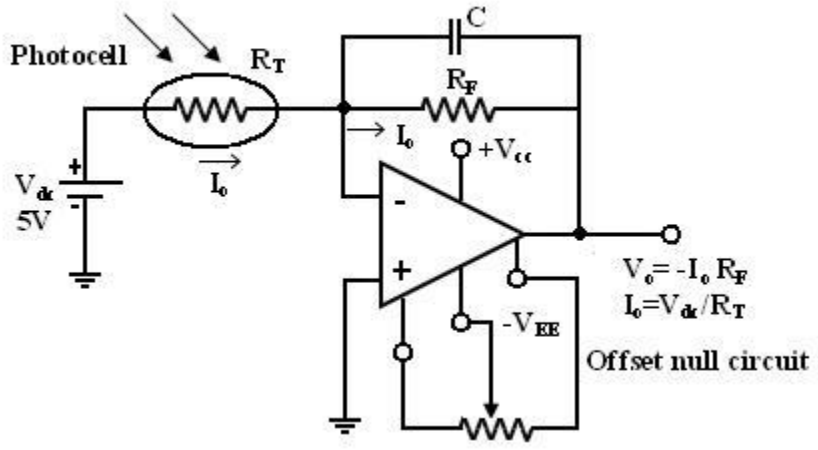
This means I_0 is zero when all inputs are logic 0.

I_0 is max when all inputs are logic 1.

The variations in I_0 can be converted into a desired o/p voltage range by selecting a proper value for R_F. since, $V_0 = I_0 R_F$

Where I_0 is given by eqn (1). It is common to parallel R_F with capacitance C to minimize the overshoot. In the fig the o/p voltage of the current to voltage converter is positive because the direction of input current I_0 is opposite to that in the basic I – V Converter.

2. Detecting current through photosensitive devices:



Photocells, photodiodes, photovoltaic cells give an output curren that depends on the intensity of light and independent of the load. The current through this devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer, it requires an external dc voltage(Vdc). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self generating circuit because it doesnot require dc voltage externally. Ex of Photovoltaic Cell : used in space applications and watches.

3.4 Summing Amplifier:

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer.

An inverting summer or a non-inverting summer may be discussed now.

3.1.13 Inverting Summing Amplifier:

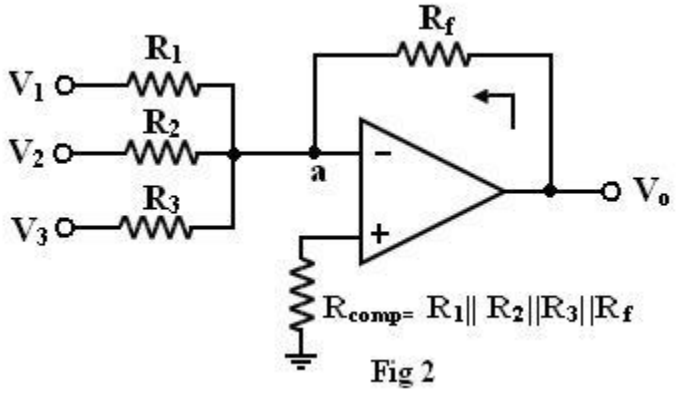


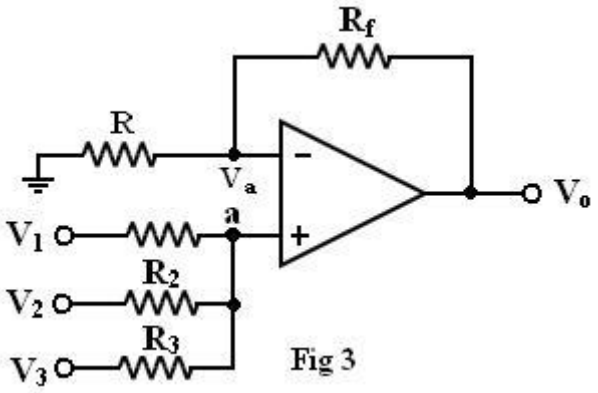
Fig 2

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$. Therefore, $R_{comp} = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$.

3.1.14 Non-Inverting Summing Amplifier:

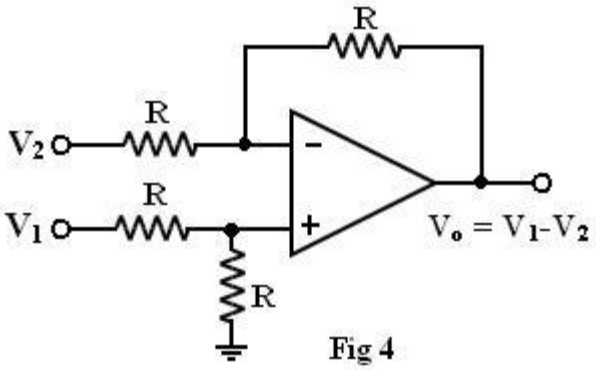


A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure 3. Let the voltage at the (-) input teriminal be V_a.

which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1+V_2+V_3$

3.5 Subtractor:



A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{01} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{01} + V_{02} = V_1 - V_2$$

3.6 Adder/Subtractor:

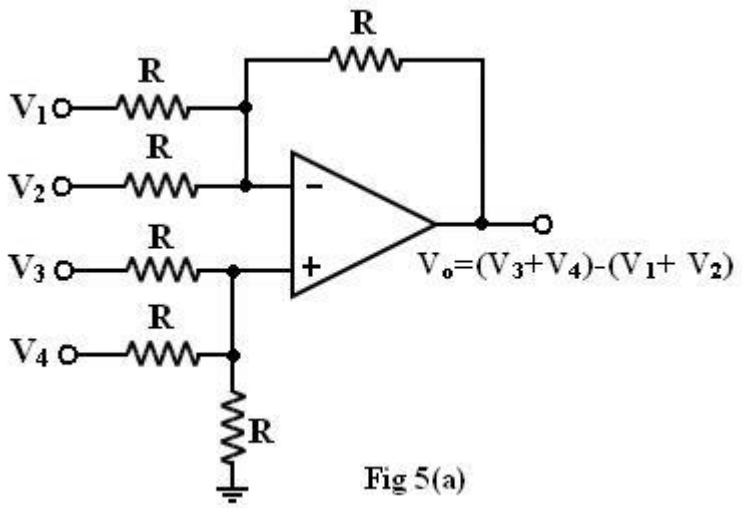


Fig 5(a)

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus, the output voltage V_o due to all four input voltages is given by

$$V_o = V_{01} + V_{02} + V_{03} + V_{04}$$

$$V_o = \frac{@V_1}{b} \frac{@V_2}{c} + V_3 + \frac{V_4}{b} \frac{}{c}$$

$$V_o = V_3 + {}_4@V_1 + V_2$$

So, the circuit is an adder-subtractor.

Instrumentation Amplifier:

The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 6(c) shows a differential instrumentation amplifier using Transducer Bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.

The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1=V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are number differential applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, and light intensity meter to name a few.

3.1.17 Differentiator:

One of the simplest of the op-amp circuits that contains capacitor in the differentiating amplifier.

Differentiator:

As the name implies, the circuit performs the mathematical operation of differentiation (i.e) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 .

The expression for the output voltage can be obtained KCL eqn written at node V_2 as follows,

Since the differentiator performs the reverse of the integrator function.

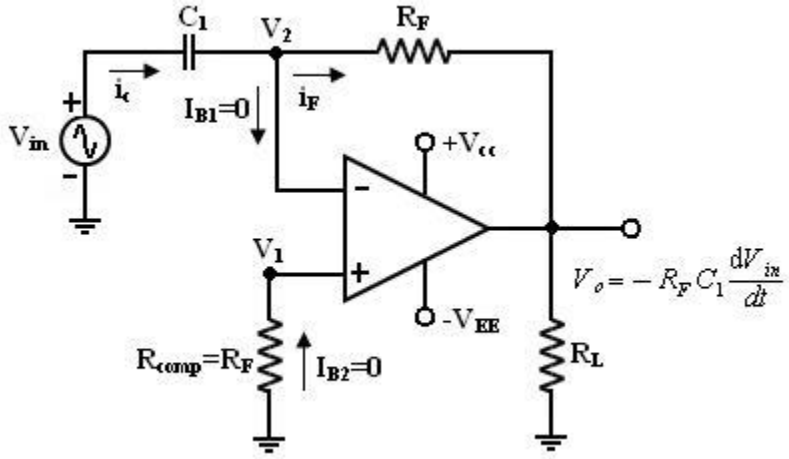
Thus the output V_0 is equal to R_F C_1 times the negative rate of change of the input voltage Vin with time.

The –sign => indicates a 180^0 phase shift of the output waveform V_0 with respect to the input signal.

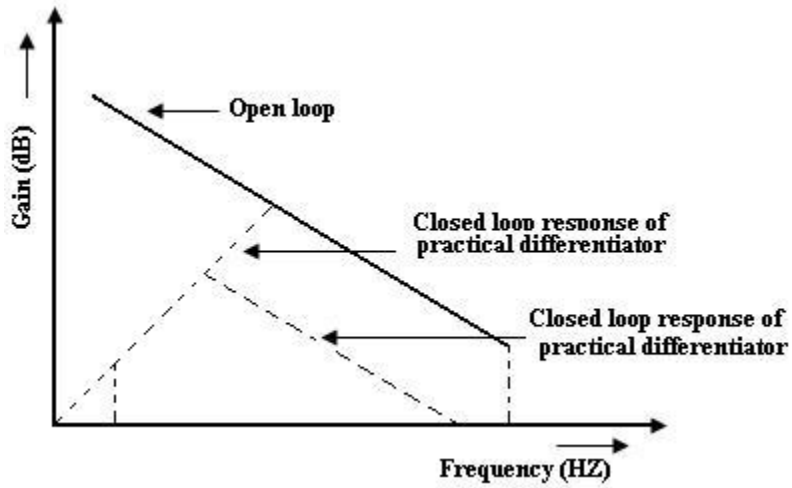
The below circuit will not do this because it has some practical problems.

The gain of the circuit (R_F /XC_1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable.

Also input impedance XC_1 S with Rin frequency which makes the circuit very susceptible to high frequency noise.



3.1.18 Basic Differetntiator



From the above fig, f_a = frequency at which the gain is 0dB and is given by, Both stability and high frequency noise problems can be corrected by the addition of 2 components. R_1 and C_F . This circuit is a practical differentiator.

From Frequency f to feedback the gain Rs at 20dB/decade after feedback the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the R_1 C_1 and R_F C_F combinations. The gain limiting frequency f_b is given by, Where R_1 C_1 = R_F C_F

R_1 C_1 and R_F C_F => helps to reduce the effect of high frequency input, amplifier noise and offsets.

All R_1 C_1 and R_F C_F make the circuit more stable by preventing the Rin gain with frequency. Generally, the value of Feedback and in turn R_1 C_1 and R_F C_F values should be selected such that

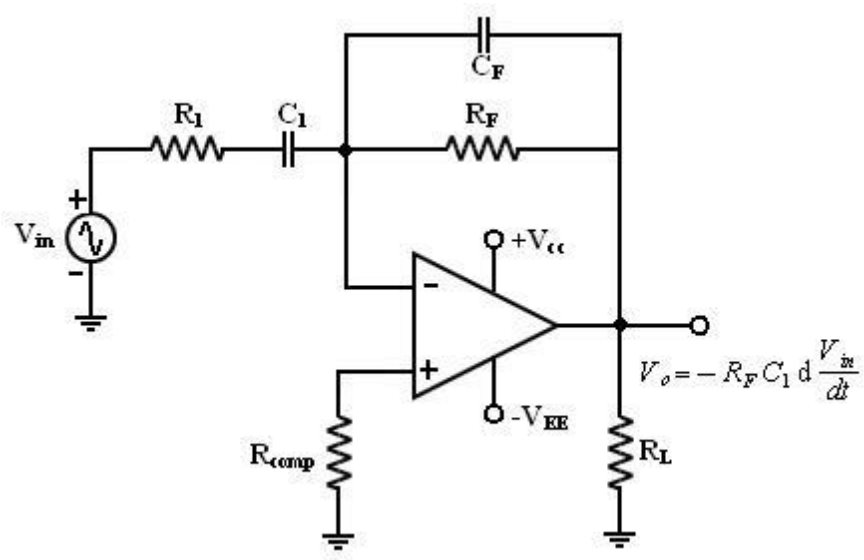
` a

$f_a < f_b < f_C$ @@@@ 2

where

f_c = *unity gain bandwidth*

The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to R_F C_1 (i.e) T > R_F C_1



3.1.19 Practical Differentiator

A workable differentiator can be designed by implementing the following steps.

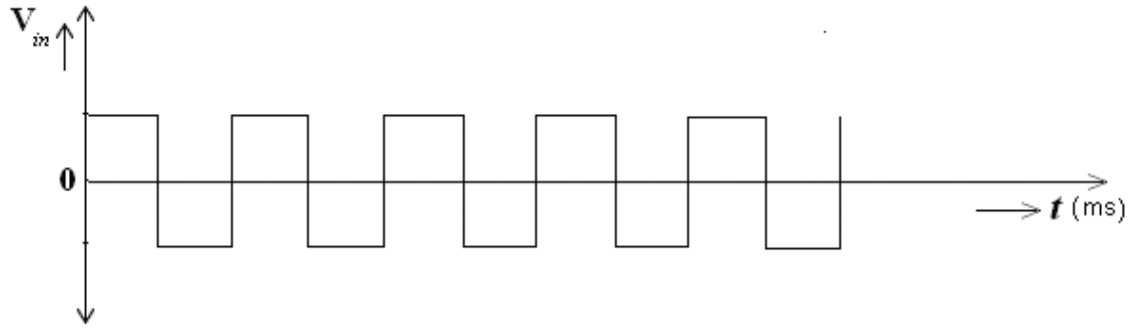
1. Select fa equal to the highest frequency of the input signal to be differentiated then assuming a value of C_1 < 1μf. Calculate the value of R_F .

2. Choose fb = 20fa and calculate the values of R_1 and C_F so that R_1 C_1 = R_F C_F .

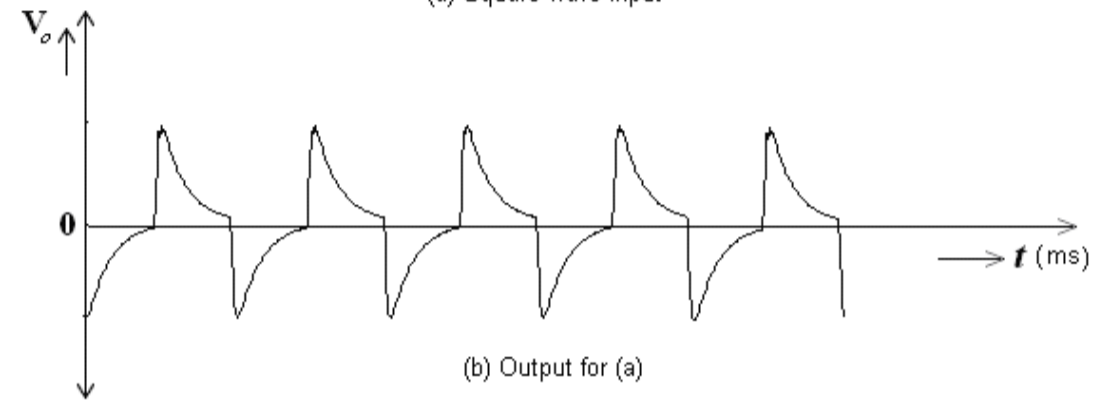
Uses:

Its used in waveshaping circuits to detect high frequency components in an input signal and also as a rate of change and detector in FM modulators.

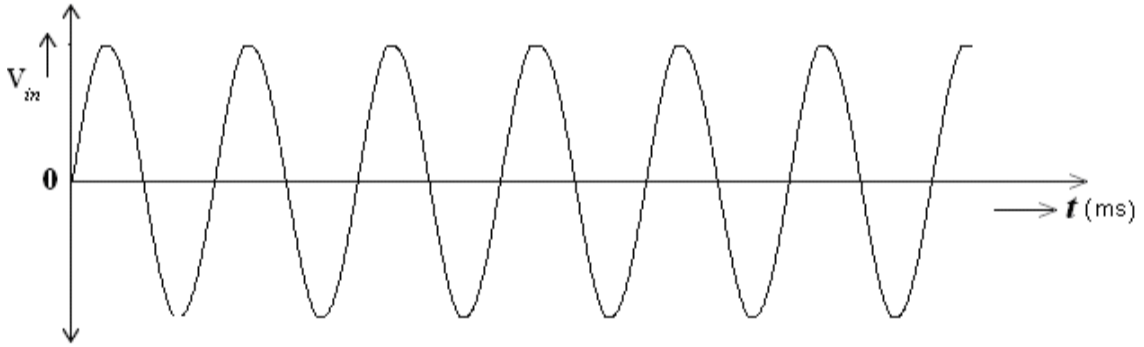
This o/p for practical differentiator



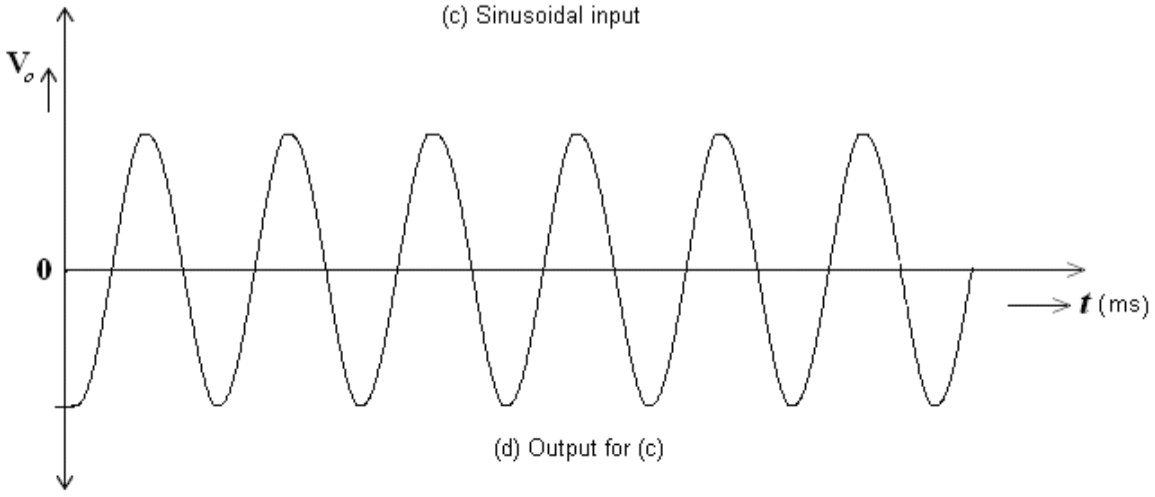
(a) Square wave input



(b) Output for (a)



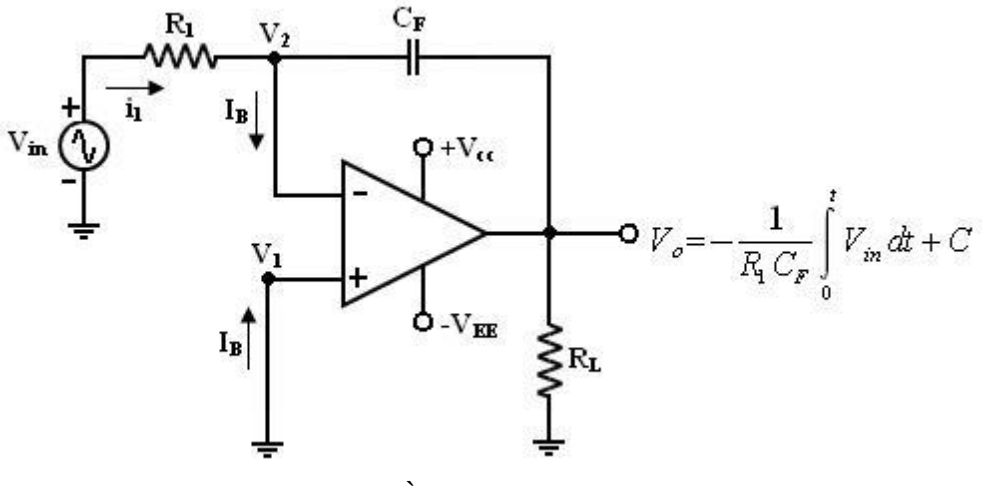
(c) Sinusoidal input



(d) Output for (c)

3.2.1 Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F . The expression for the output voltage V_0 can be obtained by KVL eqn at node V_2 .

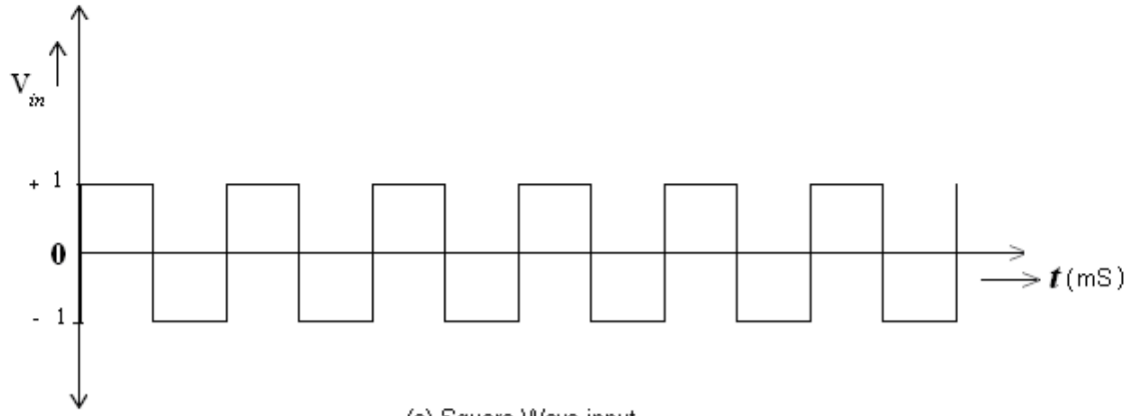


a

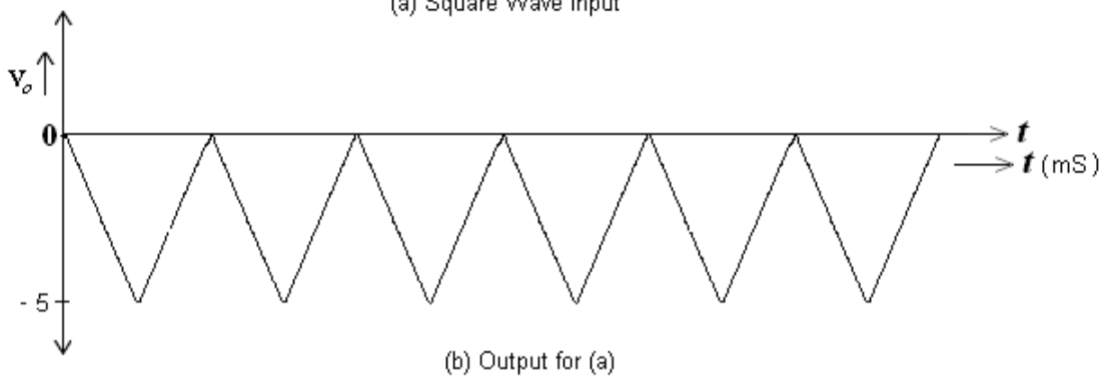
where C integration *constant* A

eqn (3) indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant $R_1 C_F$. Ex: If the input is sine wave -> output is cosine wave.

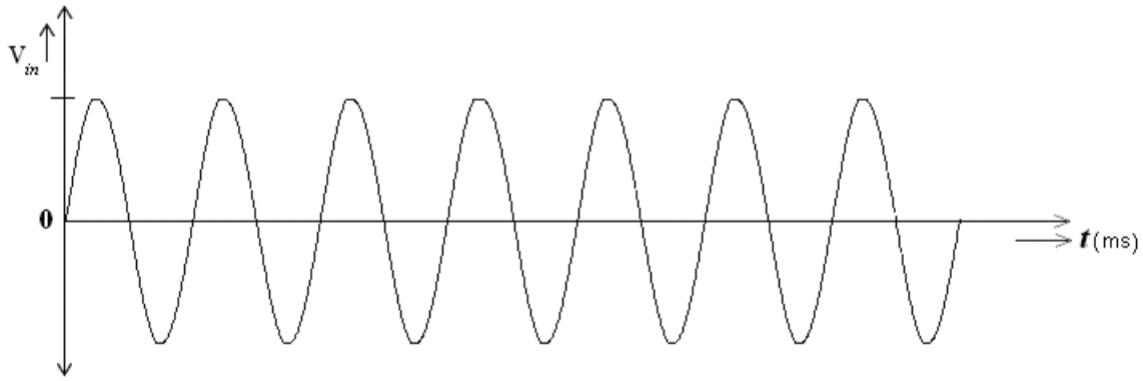
If the input is square wave -> output is triangular wave.



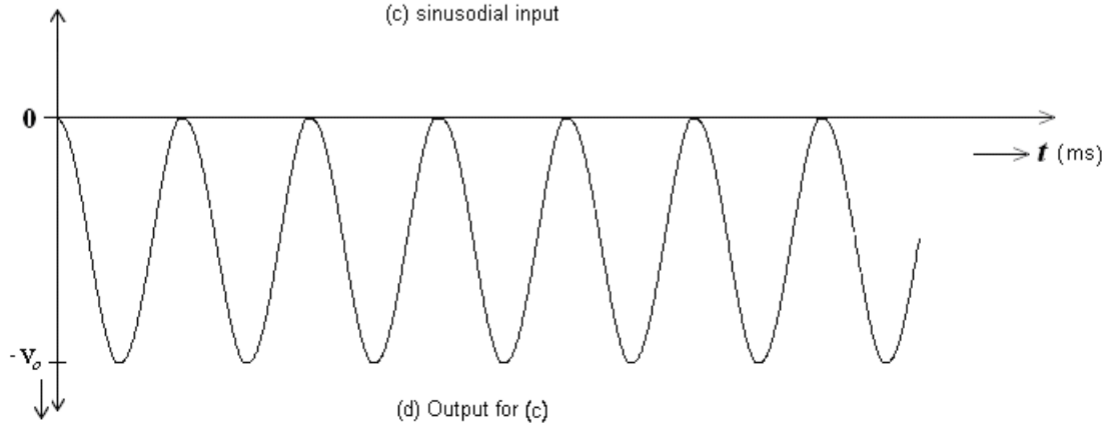
(a) Square Wave input



(b) Output for (a)



(c) sinusodial input



(d) Output for (c)

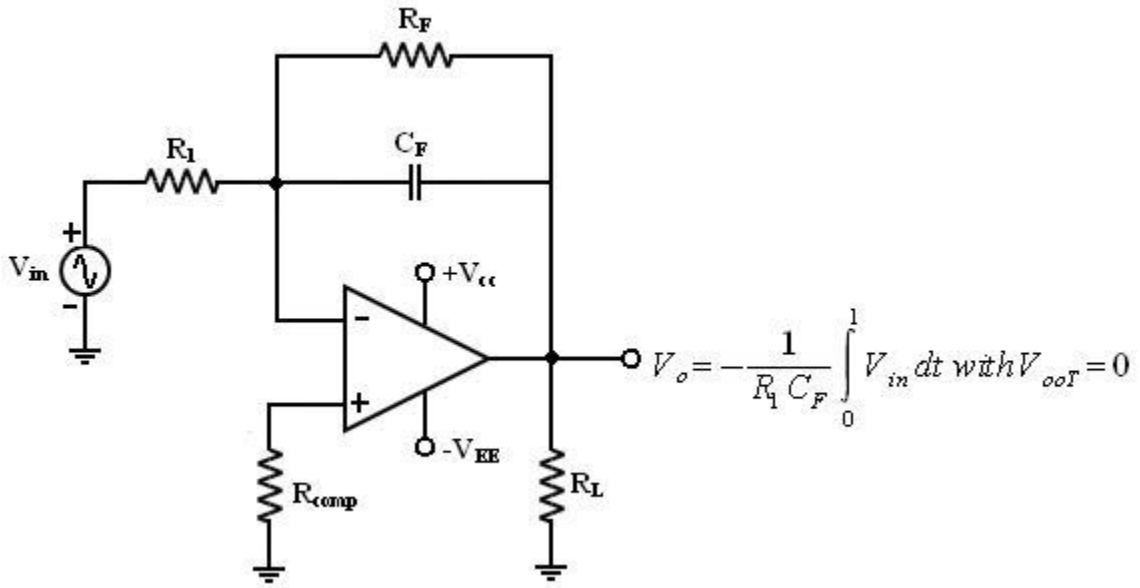
These waveform with assumption of $R_1 C_f = 1$, Vout =0V (i.e) C =0.

When Vin = 0 the integrator works as an open loop amplifier because the capacitor C_F acts an open circuit to the input offset voltage Vio.

Or

The Input offset voltage Vio and the part of the input are charging capacitor C_F produce the error voltage at the output of the integrator.

3.2.2 Practical Integrator:



Practical Integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F .

Thus R_F limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by,

Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor R_F in the practical integrator.

Stability -> refers to a constant gain as frequency of an input signal is varied over a certain range.

Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.

From the fig of practical Integrators,

f is some relative operating frequency and for frequencies f to fa to gain R_F / R_1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.

Generally the value of fa and in turn $R_1 C_F$ and $R_F C_F$ values should be selected such that fa<fb. In fact, the input signal will be integrated properly if the time period T of the signal is larger than

or

equal to $R_F C_F$, (i.e) $T \geq R_F C_F$ @@@@ 6

Uses:

Most commonly used in analog computers.

ADC

Signal wave shaping circuits.

3.2.3 Log and Antilog Amplifier:

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or Sinhx.

These can be performed continusely with log amps, and also used for direct dB display on a digital Voltmeter and Spectrum analyzer.

Log-amp can also be used to compress the dynamic range of a signal.

3.2.4 Log Amplifier:

The fundamental log amp circuit shown in fig

Fig a. Fundamental log-amp Circuit

Where a grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path. The circuit have one problem.The emitter saturation current Is varies from transistor to transistor and with temperature. Thus a stable reference voltage V ref cannot be obtaine This is eliminated by the circuit given in fig(b) The input is applied to one log-amp, while a reference voltage is applied to one log- amp,while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking. Fig(b)Log-amp with saturation current and temperature compensation

Assume $I_{S1}=I_{S2}=I$

3.2.5 Antilog Amplifier

The Circuit is shown in fig.The input Vi for the antilog-amp is fed into the temperature

compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

Since the base of Q_1 is tied to ground, we get

Or, $kT\ R_2 + R_{TC} \qquad V_{ref}$

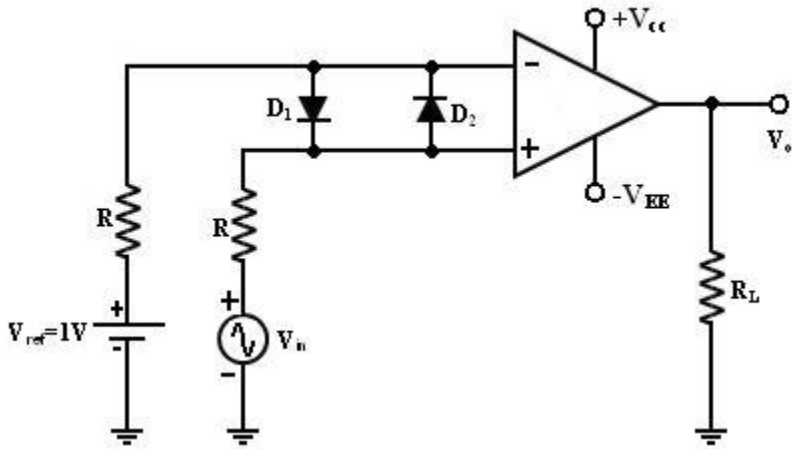
Changing the natural log i.e.,ln to $\log_{10}$ using eqn(6) we get Hence an increase of input by one volt causes the output to decrease by a decade

3.2.6 Comparator

To obtain for better performance, we shall also look at integrated designed specifically as comparators and converters. A comparator as its name implies, compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

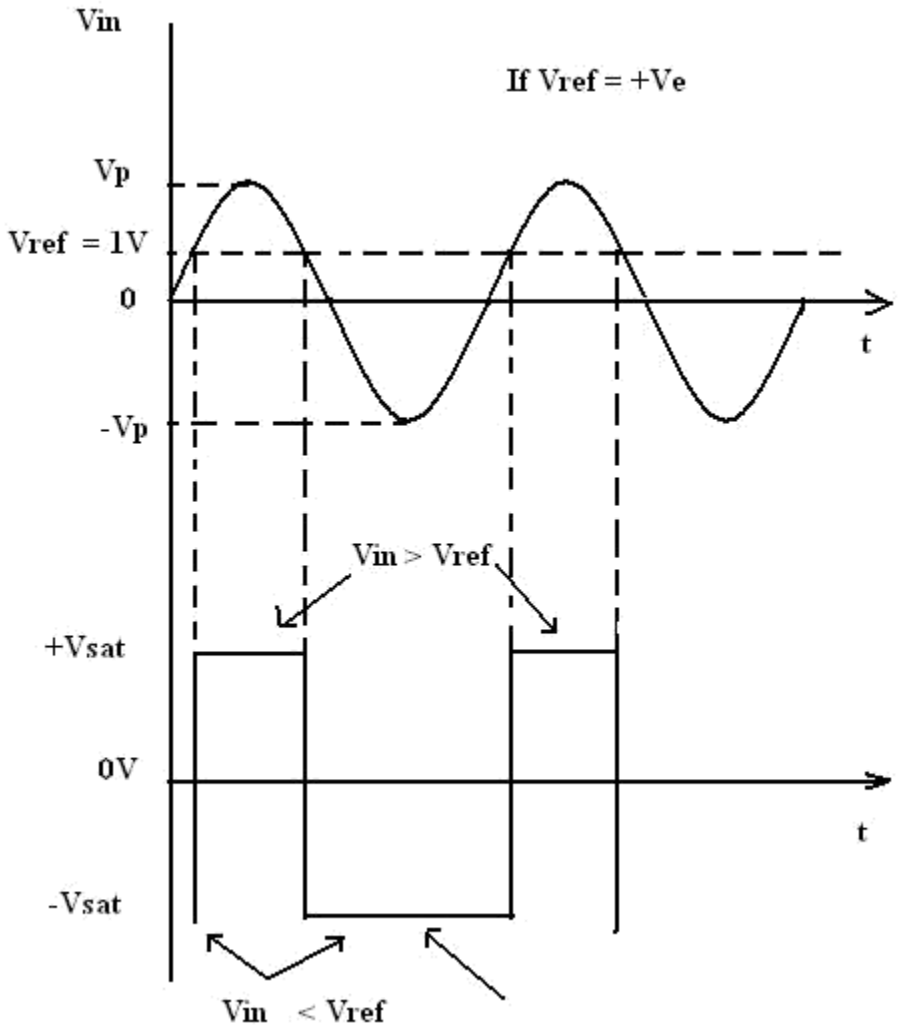
Digital Interfacing Schmitt Trigger DiscriminatoVoltage level detector and oscillators

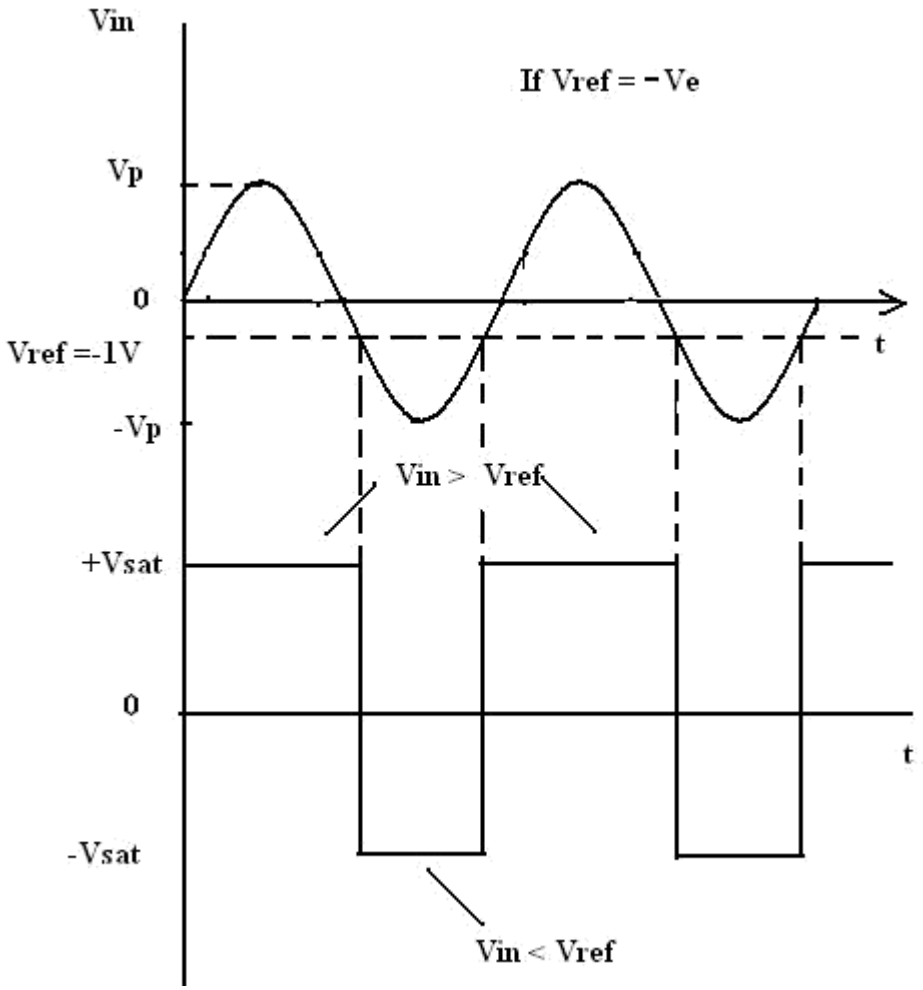
1. Non-inverting Comparator:



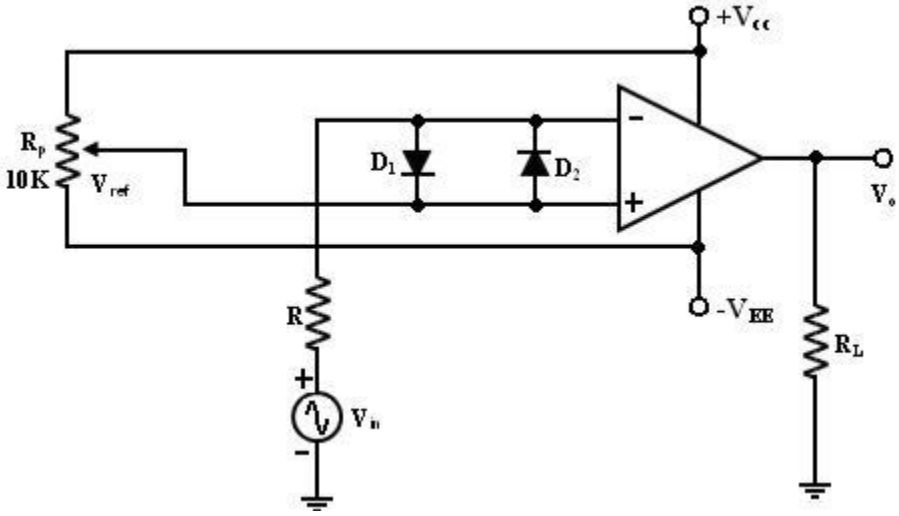
A fixed reference voltage Vref of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied tot the positive terminal.When Vin is less than Vref the output becomes V_0 at –Vsat [Vin < Vref => V_0 (-Vsat)]. When Vin is greater than Vref, the (+) input becomes positive, the V_0 goes to +Vsat. [Vin > Vref => V_0 (+Vsat)]. Thus the V_0 changes from one saturation level to another. The diodes D_1 and D_2 protects the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes. The resistance R in series with Vin is used to limit the current through D_1 and D_2 . To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and Vref.

Input and Output Waveforms:


Vin
If Vref = +Ve
Vp
Vref = 1V
0
t
-Vp
Vin > Vref
+Vsat
0V
t
-Vsat
Vin < Vref

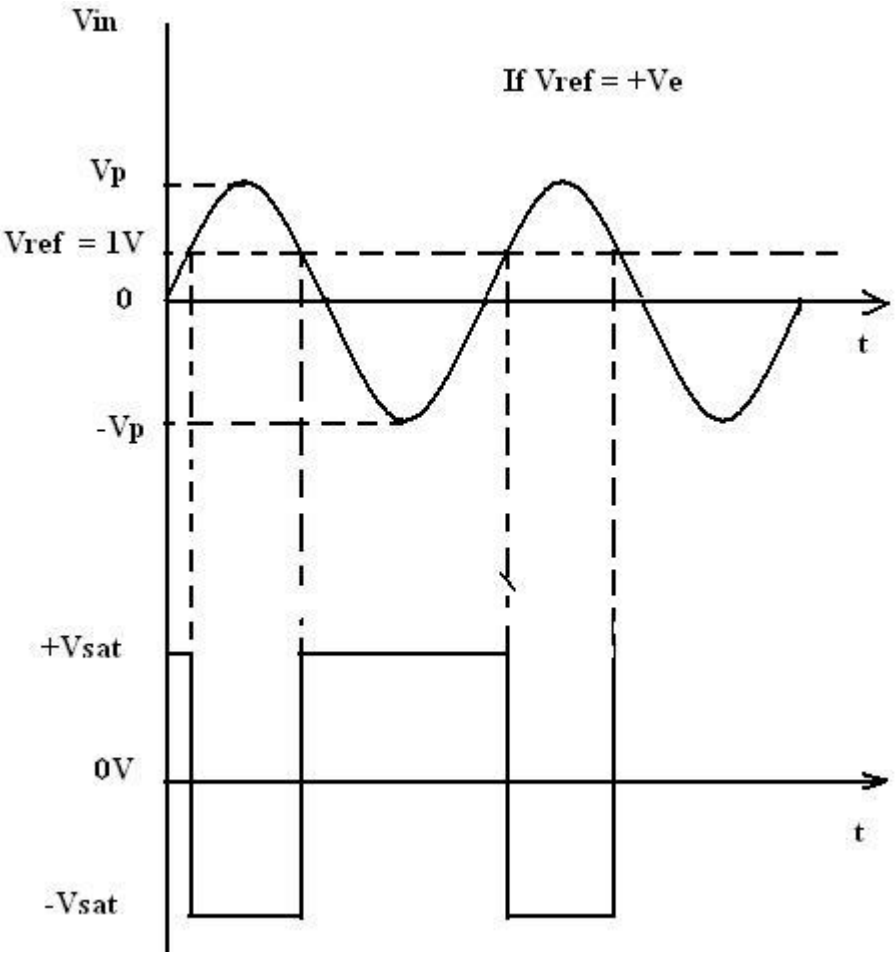


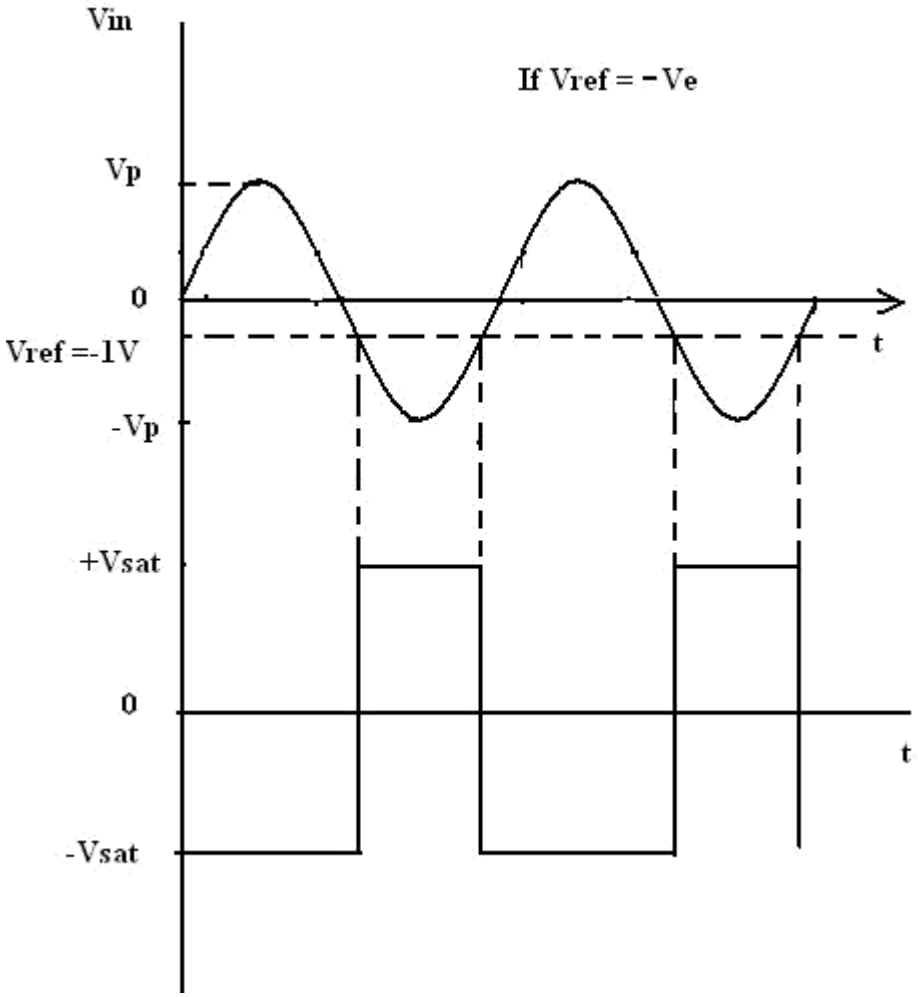
2. Inverting Comparator:



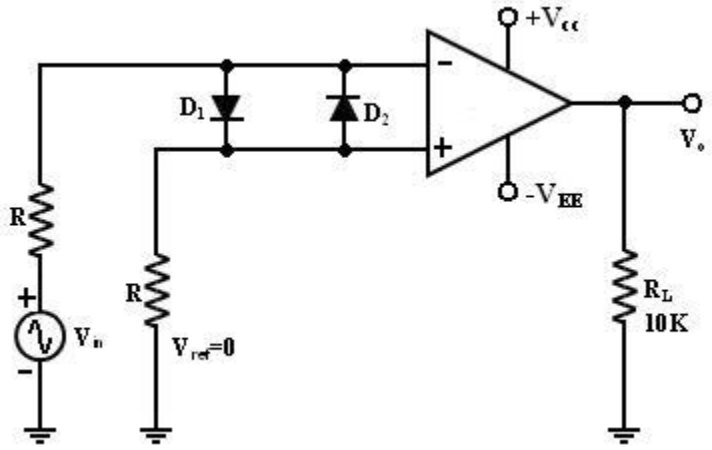
This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) input terminal and Vin is applied to the (-) input terminal. In this circuit Vref is obtained by using a

10K potentiometer that forms a voltage divider with dc supply volt +Vcc and -1 and the wiper connected to the input. As the wiper is moved towards +Vcc, Vref becomes more positive. Thus a Vref of a desired amplitude and polarity can be obtained by simply adjusting the 10k potentiometer.



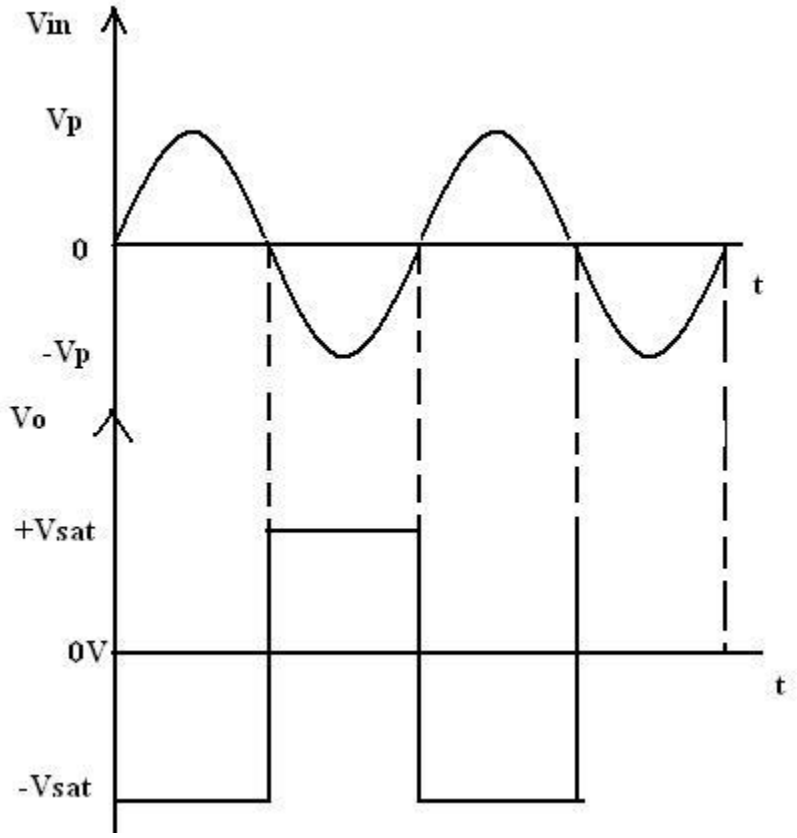


3. Zero Crossing Detector: [Sine wave to Square wave converter]



One of the application of comparator is the zero crossing detector or ―sine wave to Square wave Converter . The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero. (Vref =0V).

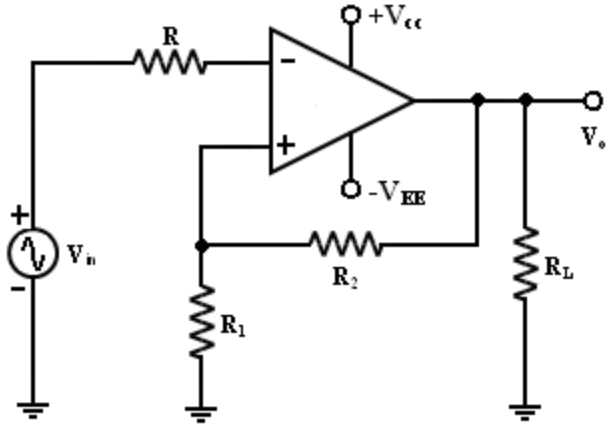
This Fig shows when in what direction an input signal Vin crosses zero volts. (i.e) the o/p V_0 is driven into negative saturation when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V_0 switches and saturates positively.

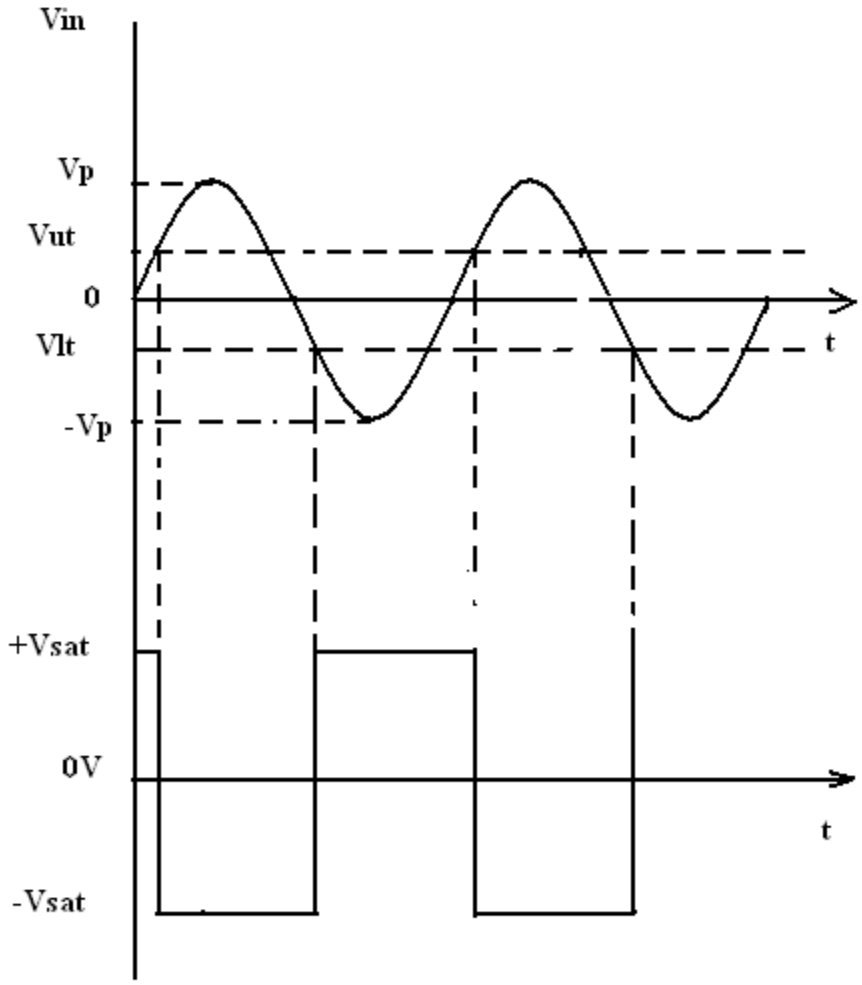


3.2.7 Drawbacks of Zero- crossing detector:

In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V_0 may not switch quickly from one saturation voltage to the other. Because of the noise at the op-amp‘s input terminals the output V_0 may fluctuate between 2 saturations voltages +Vsat and –Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V_0 to change faster and eliminate any false output transitions due to noise signals at the input. Inverting comparator with positive feedback . This is known as ―Schmitt Trigger .

Schmitt Trigger: [Square Circuit]





This circuit converts an irregular shaped waveform to a square wave or pulse. The circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers

(changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage. These threshold voltages are obtained by using theh voltage divider R_1 – R_2, where the voltage across R_1 is feedback to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value of the output voltage. When V_0 = +Vsat, the voltage across R_1 is called —upper threshold voltage Vut. The input voltage Vin must be more positive than Vut in order to cause the output V_0 to switch from +Vsat to –Vsat. As long as Vin < Vut , V_0 is at +Vsat, using voltage divider rule,

V_0 is at –Vsat. V_{lt} is given by the following eqn.

Thus, if the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions. Also the positive feedback, because of its regenerative action, will make V_0 switch faster between +Vsat and –Vsat. Resistance Rcomp t $R_1 \parallel R_2$ is used to minimize the offset problems. The comparator with positive feedback is said texhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its output switches from +Vsat to –Vsat and reverts to its original state, +Vsat when the input goes below Vlt. The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore

UNIT IV

4.1.1 THE 555 TIMER IC

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable (one - shot) multivibrator or

(ii) Astable (free running) multivibrator

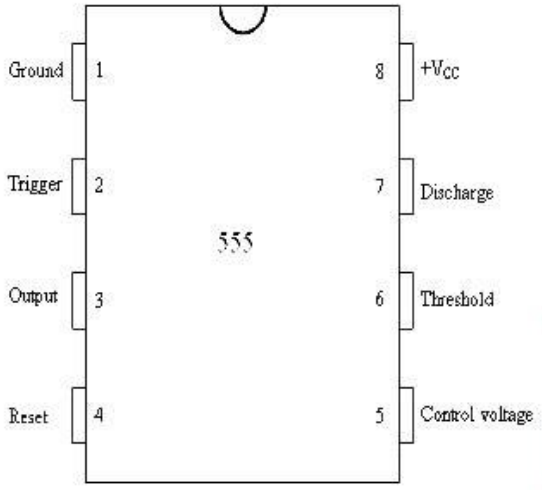
(i) It operates on +5v to +18 v supply voltages

(ii) It has an adjustable duty cycle

(iii) Timing is from microseconds to hours

(iv) It has a current o/p

PIN CONFIGURATION OF 555 TIMER:



Pin description: Pin 1: Ground:

All voltages are measured with respect to this terminal.

Pin 2: Trigger:

The o/p of the timer depends on the amplitude of the external trigger pulse applied

to this pin.

Pin 3: Output:

There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage

(Between Pin 3 & Ground ➔ ON load) (Between Pin 3 & + Vcc ➔ OFF load)

(i) When the input is low:

The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

(ii) When the output is high:

The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This

current is called the source current.

Pin 4: Reset:

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage:

An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold:

This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge:

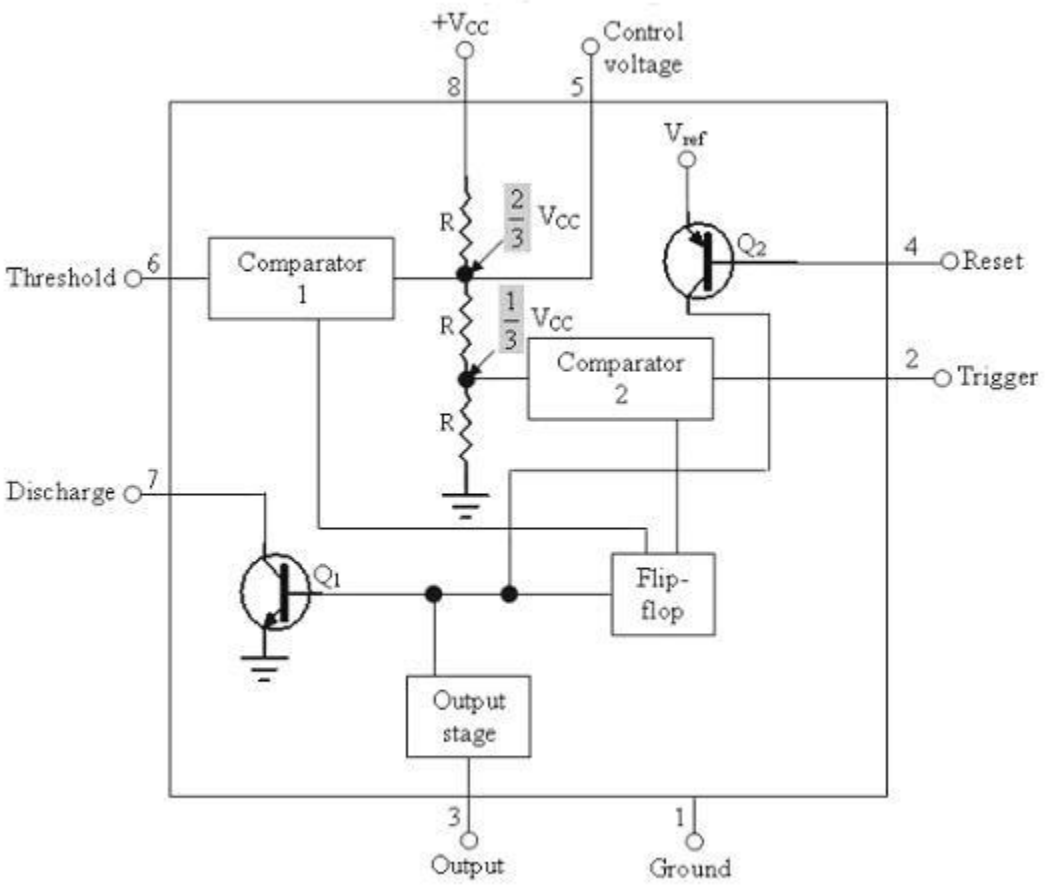
This pin is connected internally to the collector of transistor Q1.

When the output is high Q1 is OFF.

When the output is low Q is (saturated) ON.

Pin 8: +Vcc: The supply voltage of +5V to +18V is applied to this pin with respect to ground.

4.1.2 Block Diagram of 555 Timer IC:



From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).

(i) In the Stable state:

The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

(ii) At the Negative going trigger pulse:

The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q=1; Q=0

(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; Q = 1 The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

Monostable Operation:

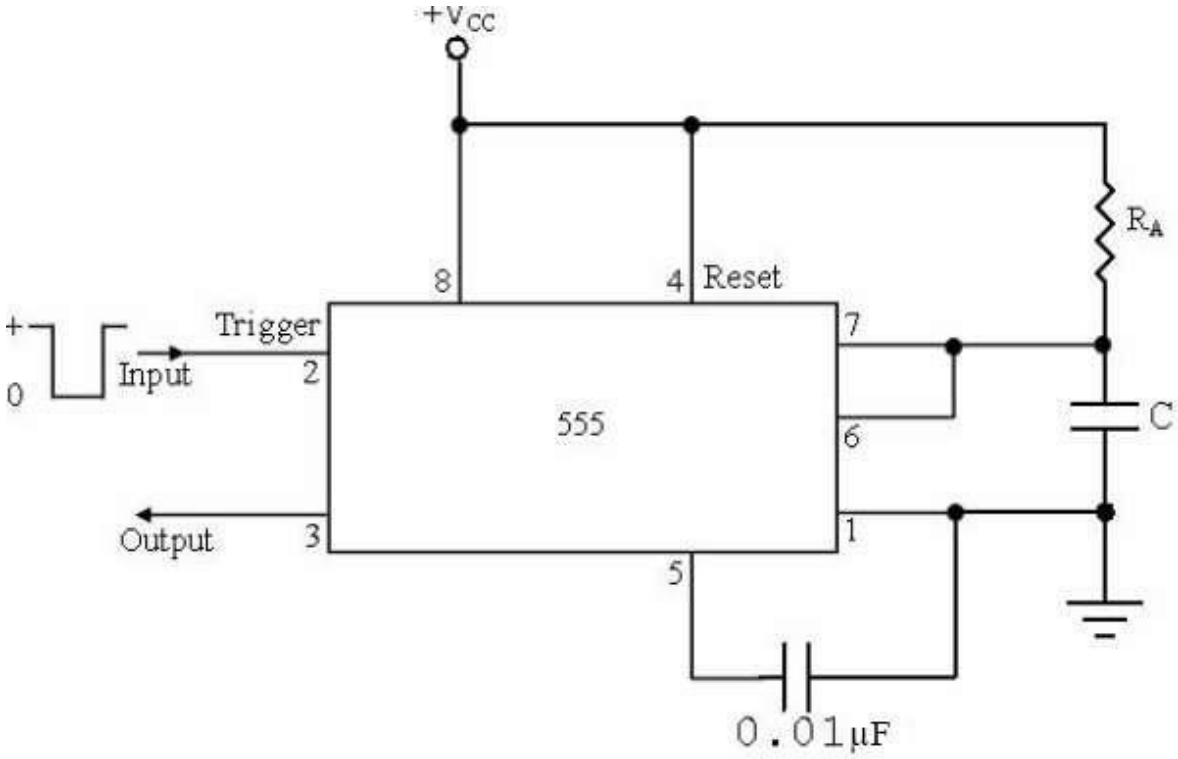
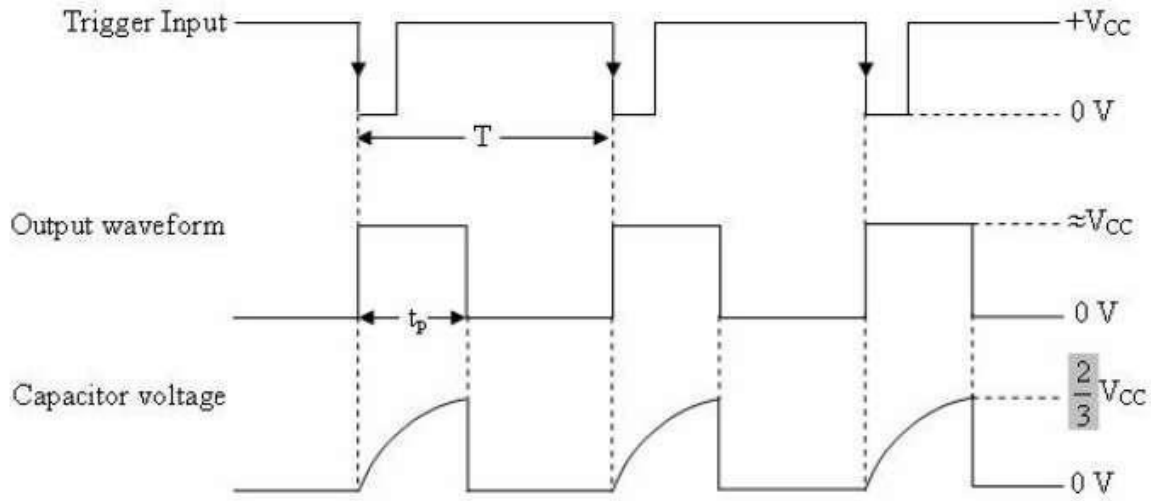
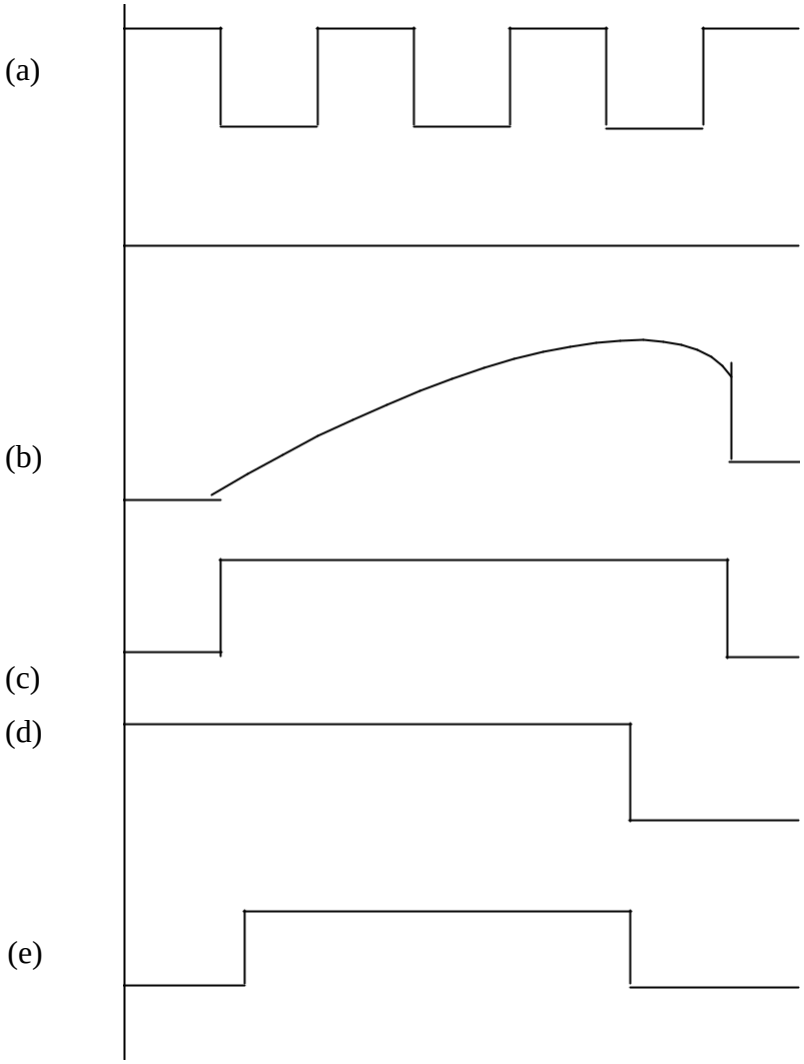


Fig : 555 connected as a Monostable Multivibrator

Model Graph:



Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through R_A. When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.



Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (fig b) as shown in below. After the time period, the upper comparator resets the FF, i.e. Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential (fig c)]. The voltage across the capacitor as in fig (b) is given by

$$Vc = Vcc\,(1-e^{-t/RC}) \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Therefore At t = T, Vc = 2/3 Vcc

$$2/3\ Vcc = Vcc(1-e^{-T/RC})$$

or

$$T = RC \ln (1/3)$$

Or

$$T = 1.1RC \text{ seconds} \qquad \ldots\ldots\ldots\ldots\ldots (2)$$

If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

4.1.3 Applications of Monostable Mode of Operation: (a) Frequency Divider:

The 555 timer as a monostable mode. It can be used as a frequency divider by adjusting the length of the timing cycle t_p with respect to the time period T of the trigger input. To use the monostable multivibrator as a divide by 2 circuit, the timing interval t_p must be a larger than the time period of the trigger input. [Divide by 2 ➔ $t_p > T$ of the trigger] By the same concept, to use the monostable multivibrator as a divide by 3 circuit, t_p must be slightly larger than twice the period of the input trigger signal & so on, [divide by 3 ➔ $t_p > 2T$ of trigger]

(b) Pulse width modulation:

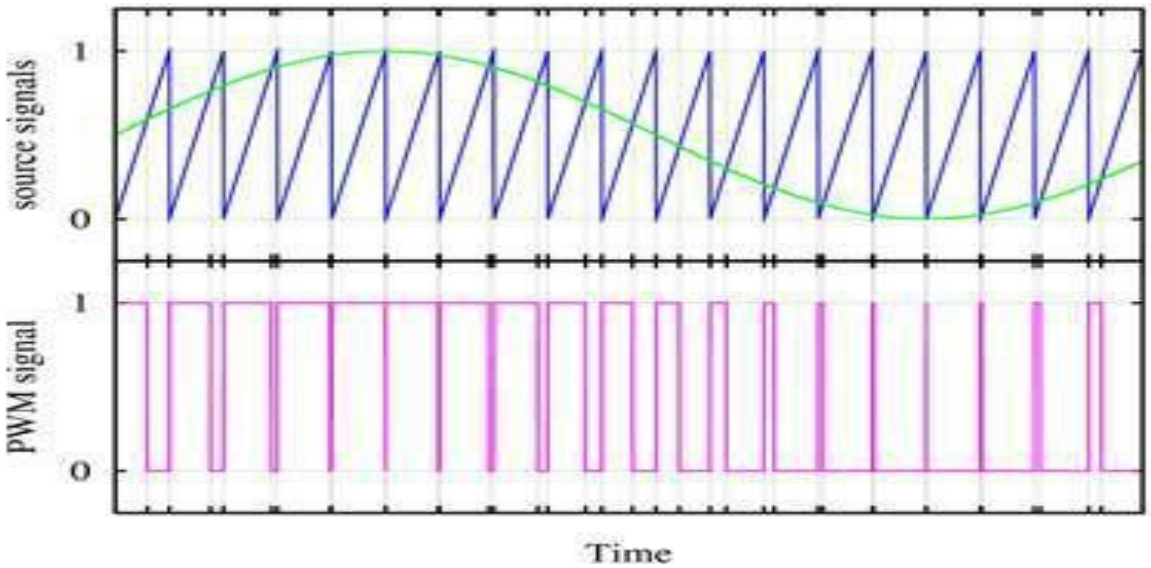


Fig: Pulse Width Modulation Output Waveform

Pulse width of a carrier wave changes in accordance with the value of a incoming (modulating signal) is known as PWM. It is basically monostable multivibrator. A modulating signal is fed in to the control voltage (pin 5). Internally, the control voltage is adjusted to 2/3 Vcc externally applied modulating signal changes the control voltage level of upper comparator. As a result, the required to change the capacitor up to threshold voltage level changes, giving PWM output.

(c) Pulse Stretcher:

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name ― Pulse stretcher‖. Often, narrow –pulse width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to the eye because its on time is infinitesimally small compared to its off time. The 55 pulse stretcher can be used to remedy this problem. The LED will be ON during the timing interval $t_p = 1.1R_AC$ which can be varied by changing the value of R_A & C.

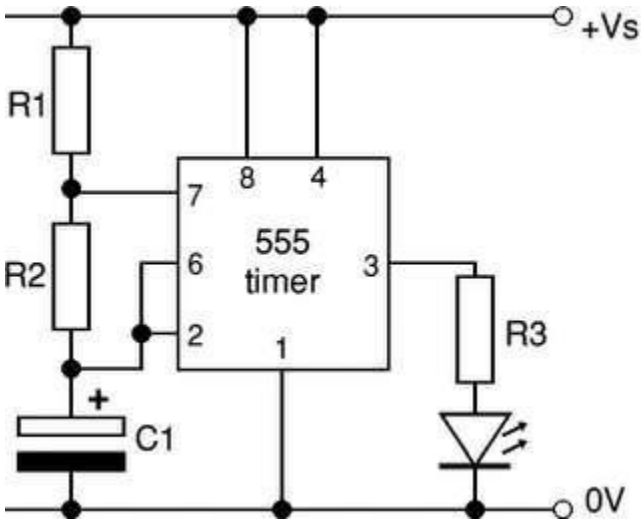
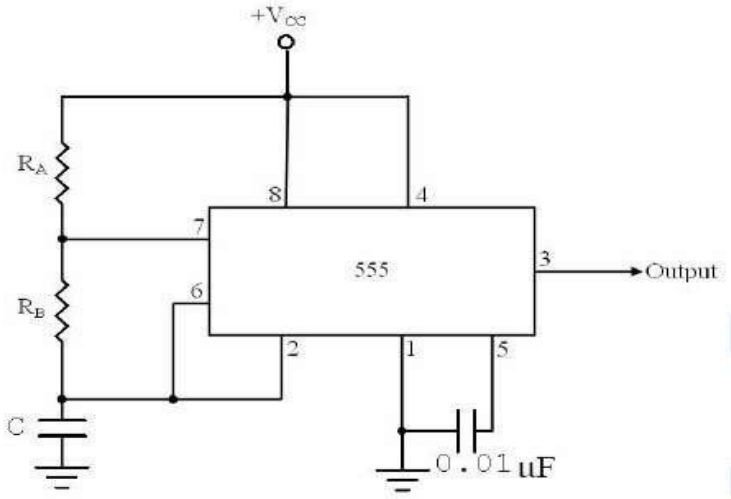


Fig: Pulse Stretcher

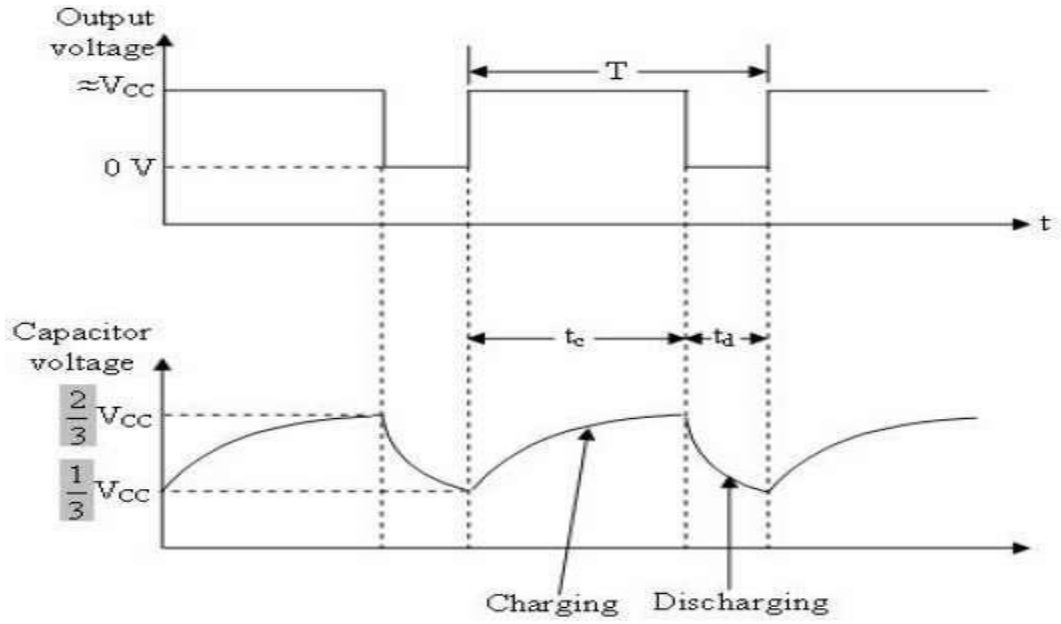
4.1.4 The 555 timer as an Astable Multivibrator:

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 55 timer.

Fig: Astable Multivibrator



Model Graph



The above figures show the 555 timer connected as an astable multivibrator and its model graph

Initially, when the output is high :Capacitor C starts charging toward Vcc through R_A & R_B. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through R_B and transistor Q1, when the voltage across C equals 1/3

Vcc, lower comparator output triggers the FF & the output goes High. Then cycle repeats. The

capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high &

is given by

$$t_c = (R_A+R_B)C \ln 2 \ldots\ldots\ldots\ldots (1) \text{ Where } [\ln 2 = 0.69]$$

$$= 0.69 (R_A+R_B)C$$

Where R_A & R_B are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

$$t_c = R_B C \ln 2$$

$$t_d = 0.69 R_B C \ldots\ldots\ldots\ldots\ldots\ldots..(2)$$

where R_B is in ohms and C is in farads.

Thus the total period of the output waveform is

$$T = t_c + t_d = 0.69 (R_A+2R_B)C \ldots\ldots\ldots\ldots\ldots(3)$$

This, in turn, gives the frequency of oscillation as, $f_0 = 1/T = 1.45/(R_A+2R_B)C \ldots\ldots\ldots(4)$

Equation 4 indicates that the frequency f_0 is independent of the supply voltage Vcc. Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed as a percentage.

% duty cycle = $(t_c / T) * 100$

% DC = $[(R_A+R_B)/ /(R_A+2R_B)] * 100$

4.1.5 Astable Multivibrator

Applications:

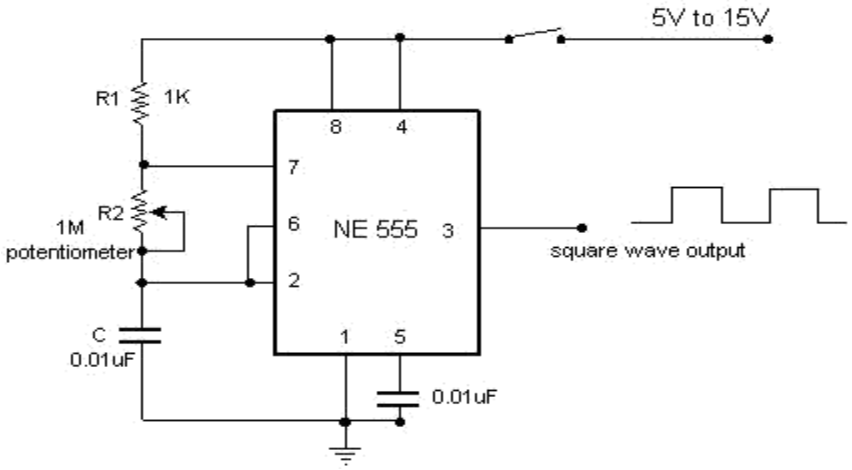


Fig: Square Wave Oscillator

With out reducing R_A = 0 ohm, the astable multivibrator can be used to produce square wave output. Simply by connecting diode D across Resistor R_B. The capacitor C charges through R_A & diode D to approximately

2/3 Vcc & discharges through R_B & Q1 until the capacitor voltage equals approximately 1/3 Vcc, then the cycle repeats.

To obtain a square wave output, R_A must be a combination of a fixed resistor & potentiometer so that the potentiometer can be adjusted for the exact square wave.

(b) Free – running Ramp generator:

- The astable multivibrator can be used as a free – running ramp generator when resistor R_A & R_B are replaced by a current mirror.
- The current mirror starts charging capacitor C toward Vcc at a constant rate.
- When voltage across **C equals to 2/3 Vcc**, upper comparator turns transistor Q1 ON & C rapidly discharges through transistor Q1.
- When voltage across **C equals to 1/3 Vcc**, lower comparator switches transistor OFF & then capacitor C starts charging up again..
- Thus the charge – discharge cycle keeps repeating.
- The discharging time of the capacitor is relatively negligible compared to its charging time.
- The time period of the ramp waveform is equal to the charging time & is approximately is given by,

$$T = VccC/3I_C \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$I_C = (Vcc - V_{BE})/R = \text{constant current}$$

Therefore the free – running frequency of ramp generator is

$$f_0 = 3I_C / V_{cc} C \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

UNIT V

5.1.1 IC VOLTAGE REGULATORS

Four most commonly used switching converter types: Buck: used the reduce a DC voltage to a lower DC voltage. Boost: provides an output voltage that is higher than the input. Buck-Boost (invert): an output voltage is generated opposite in polarity to the input. Flyback: an output voltage that is less than or greater than the input can be generated, as well as multiple outputs.Converters: Push-Pull: A two-transistor converter that is especially efficient at low input voltages. Half-Bridge:A two-transistor converter used in many off-line applications. Full-Bridge: A four-transistor converter (usually used in off-line designs) that can generate the highest output power of all the types listed. Application information will be provided along with circuit examples that illustrate some applications of Buck, Boost, and Flyback regulators.

5.2.1 Switching Fundamentals

The law of inductance

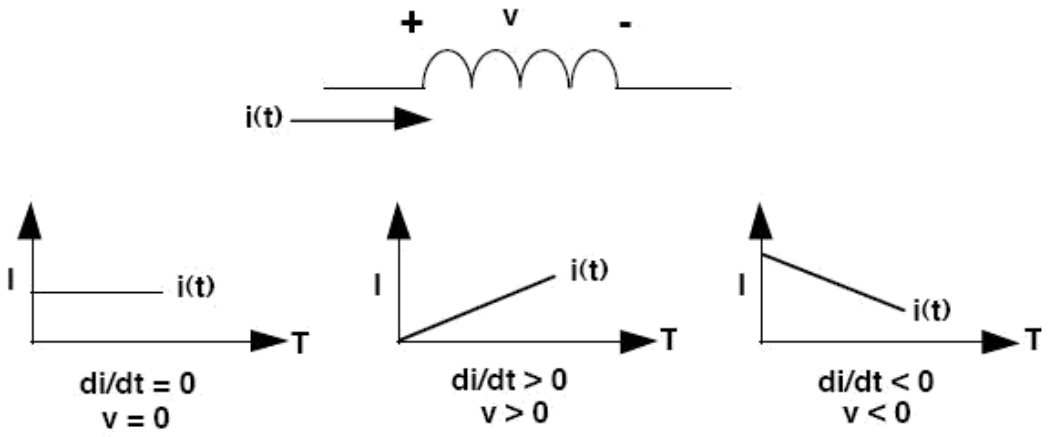
If a voltage is forced across an inductor, a current will flow through that inductor (and this current will vary with time). The current flowing in an inductor will be time-varying even if the forcing voltage is constant. It is equally correct to say that if a time-varying current is forced to flow in an inductor, a voltage across the inductor will result. The fundamental law that defines the relationship between the voltage and current in an inductor is given by the equation:

$$v = L\,(di/dt)$$

Two important characteristics of an inductor that follow directly from the law of inductance are:

1) A voltage across an inductor results only from a current that changes with time. A steady (DC) current flowing in an inductor causes no voltage across it (except for the tiny voltage drop across the copper used in the windings).

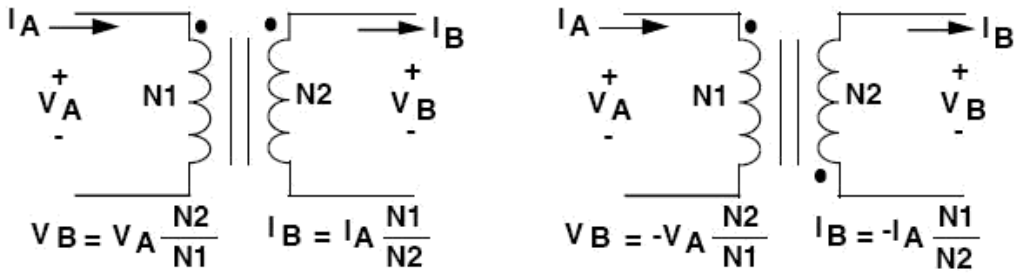
2) A current flowing in an inductor can not change value instantly (in zero time), as this would require infinite voltage to force it to happen. However, the faster the current is changed in an inductor, the larger the resulting voltage will be. Note: Unlike the current flowing in the inductor, the voltage across it can change instantly (in zero time). The principles of inductance are illustrated by the information contained in Figure.



The important parameter is the di/dt term, which is simply a measure of how the current changes with time. When the current is plotted versus time, the value of di/dt is defined as the slope of the current plot at any given point. The graph on the left shows that current which is constant with time has a di/dt value of zero, and results in no voltage across the inductor. The center graph shows that a current which is increasing with time has a positive di/dt value, resulting in a positive inductor voltage. Current that decreases with time (shown in the right-hand graph) gives a negative value for di/dt and inductor voltage. It is important to note that a linear current ramp in an inductor (either up or down) occurs only when it has a constant voltage across it.

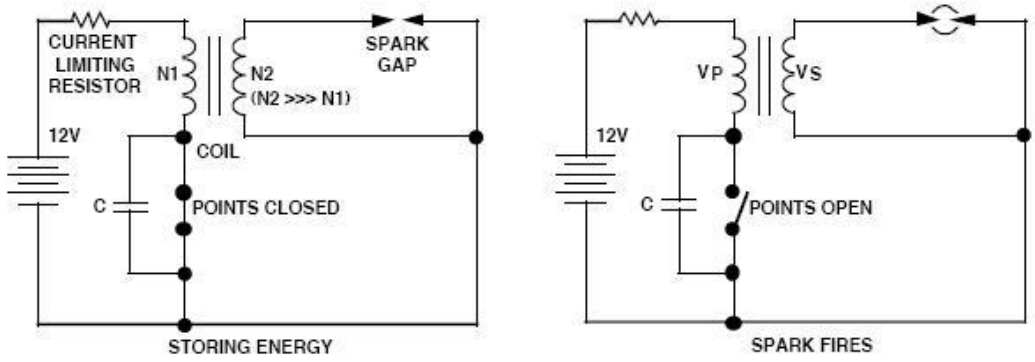
5.2.2 Transformer Operation:

A transformer is a device that has two or more magnetically-coupled windings. The basic operation is shown in Figure. The action of a transformer is such that a time-varying (AC) voltage or current is transformed to a higher or lower value, as set by the transformer turns ratio. The transformer does not add power, so it follows that the power (V X I) on either side must be constant. That is the reason that the winding with more turns has higher voltage but lower current, while the winding with less turns has lower voltage but higher current.The dot on a transformer winding identifies its polarity with respect to another winding, and reversing the dot results in inverting the polarity Example of Transformer Operation: An excellent example of how a transformer works can be found under the hood of your car, where a transformer is used to generate the 40 kV that fires car‘s spark plugs.



5.2.3 Spark Firing Circuit:

The "coil" used to generate the spark voltage is actually a transformer, with a very high secondary- to-primary turns ratio. When the points first close, current starts to flow in the primary winding and eventually reaches the final value set by the 12V battery and the current limiting resistor. At this time, the current flow is a fixed DC value, which means no voltage is generated across either winding of the transformer.



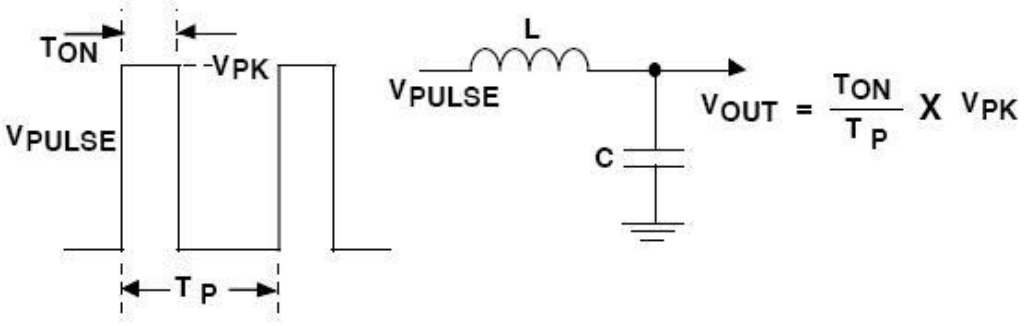
When the points open, the current in the primary winding collapses very quickly, causing a large voltage to appear across this winding. This voltage on the primary is magnetically coupled to (and stepped up by) the secondary winding, generating a voltage of 30 kV - 40 kV on the secondary side. As explained previously, the law of inductance says that it is not possible to instantly break the current flowing in an inductor (because an infinite voltage would be required to make it happen).

This principle is what causes the arcing across the contacts used in switches that are in circuits with highly inductive loads. When the switch just begins to open, the high voltage generated allows electrons to jump the air gap so that the current flow does not actually stop instantly. Placing a capacitor across the contacts helps to reduce this arcing effect. In the automobile ignition, a capacitor is placed across the points to minimize damage due to arcing when the points "break" the current flowing in the low-voltage coil winding (in car manuals, this capacitor

is referred to as a "condenser").

5.2.4 Pulse Width Modulation (PWM):

All of the switching converters that will be covered in this paper use a form of output voltage regulation known as Pulse Width Modulation (PWM). Put simply, the feedback loop adjusts (corrects) the output voltage by changing the ON time of the switching element in the converter. As an example of how PWM works, we will examine the result of applying a series of square wave pulses to an L-C filter (see Figure).

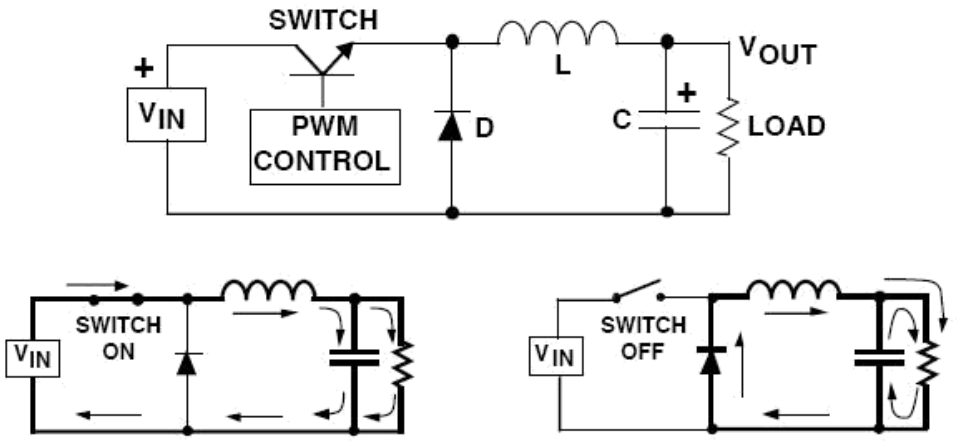


The series of square wave pulses is filtered and provides a DC output voltage that is equal to the peak pulse amplitude multiplied times the duty cycle (duty cycle is defined as the switch ON time divided by the total period). This relationship explains how the output voltage can be directly controlled by changing the ON time of the switch.

Switching Converter Topologies The most commonly used DC-DC converter circuits will now be presented along with the basic principles of operation.

5.2.5 Buck Regulator:

The most commonly used switching converter is the Buck, which is used to down-convert a DC voltage to a lower DC voltage of the same polarity. This is essential in systems that use distributed power rails (like 24V to 48V), which must be locally converted to 15V, 12V or 5V with very little power loss. The Buck converter uses a transistor as a switch that alternately connects and disconnects the input voltage to an inductor (see Figure).



The lower diagrams show the current flow paths (shown as the heavy lines) when the switch is on and off. When the switch turns on, the input voltage is connected to the inductor. The difference between the input and output voltages is then forced across the inductor, causing current through the inductor to increase. During the on time, the inductor current flows into both the load and the output capacitor (the capacitor charges during this time).

When the switch is turned off, the input voltage applied to the inductor is removed. However, since the current in an inductor can not change instantly, the voltage across the inductor will adjust to hold the current constant. The input end of the inductor is forced negative in voltage by the decreasing current, eventually reaching the point where the diode is turned on. The inductor current then flows through the load and back through the diode. The capacitor discharges into the load during the off time, contributing to the total current being supplied to the load (the total load current during the switch off time is the sum of the inductor and capacitor current).

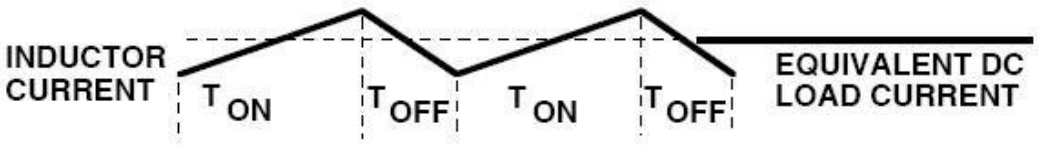


FIGURE 30. BUCK REGULATOR INDUCTOR CURRENT

The shape of the current flowing in the inductor is similar to previous figure. As explained, the current through the inductor ramps up when the switch is on, and ramps down when the switch is off. The DC load current from the regulated output is the average value of the inductor current. The peak-to-peak difference in the inductor current waveform is referred to as the inductor ripple current, and the inductor is typically selected large enough to keep this ripple current less than 20%

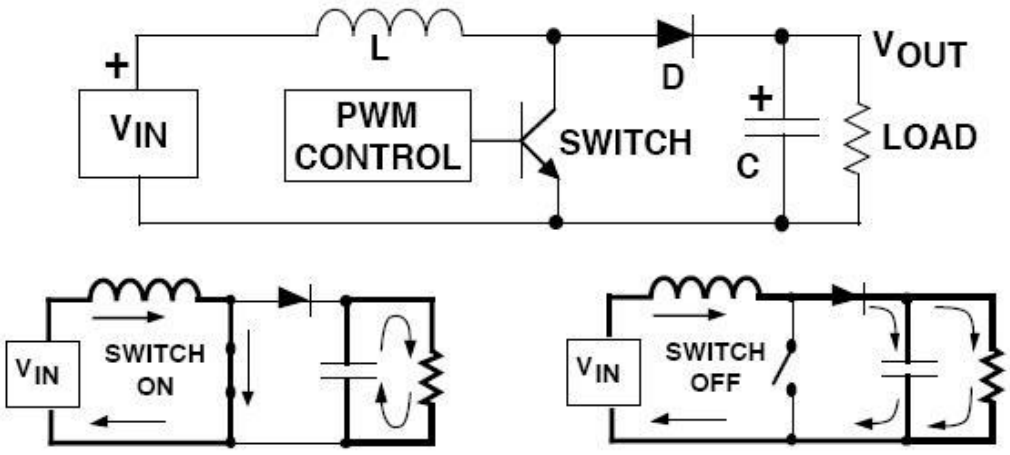
to 30% of the rated DC current.

5.2.6 Continuous vs. Discontinuous operation

In most Buck regulator applications, the inductor current never drops to zero during Full-load operation (this is defined as continuous mode operation). Overall performance is usually better using continuous mode, and it allows maximum output power to be obtained from a given input voltage and switch current rating. In applications where the maximum load current is fairly low, it can be advantageous to design for discontinuous mode operation. In these cases, operating in discontinuous mode can result in a smaller overall converter size (because a smaller inductor can be used).Discontinuous mode operation at lower load current values is generally harmless, and even converters designed for continuous mode operation at full load will become discontinuous as the load current is decreased (usually causing no problems).

5.2.7Boost Regulator:

The Boost regulator takes a DC input voltage and produces a DC output voltage that is higher in value than the input (but of the same polarity). The Boost regulator is shown in Figure, along with details showing the path of current flow during the switch on and off time. Whenever the switch is on, the input voltage is forced across the inductor which causes the current through it to increase (ramp up).



When the switch is off, the decreasing inductor current forces the "switch" end of the inductor to swing positive. This forward biases the diode, allowing the capacitor to charge up to a voltage that is higher than the input voltage. During steady-state operation, the inductor current flows into both the output capacitor and the load during the switch off time. When the switch is on, the load

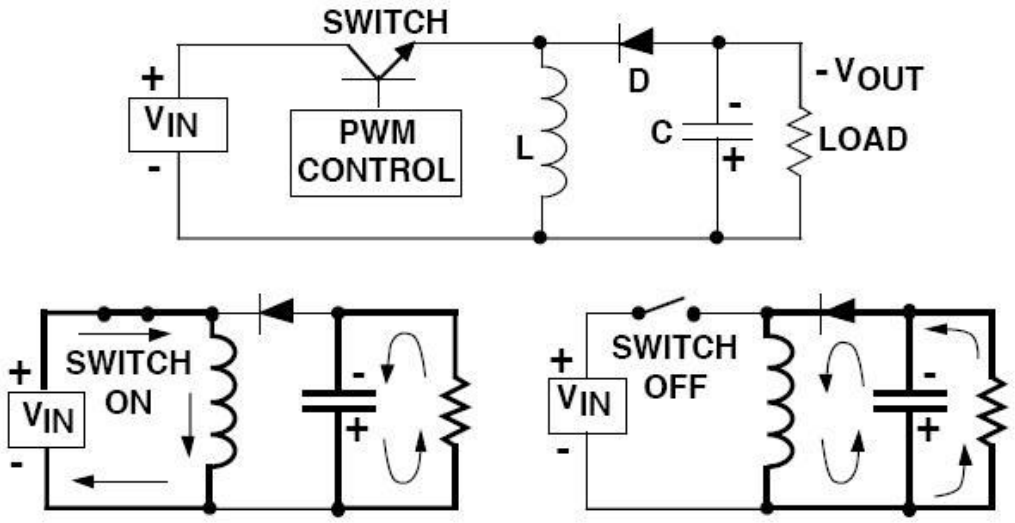
current is supplied only by the capacitor.

5.2.8 Output Current and Load power:

An important design consideration in the Boost regulator is that the output load current and the switch current are not equal, and the maximum available load current is always less than the current rating of the switch transistor. It should be noted that the maximum total power available for conversion in any regulator is equal to the input voltage multiplied times the maximum average input current (which is less than the current rating of the switch transistor). Since the output voltage of the Boost is higher than the input voltage, it follows that the output current must be lower than the input current.

5.2.9 Buck-Boost (Inverting) Regulator:

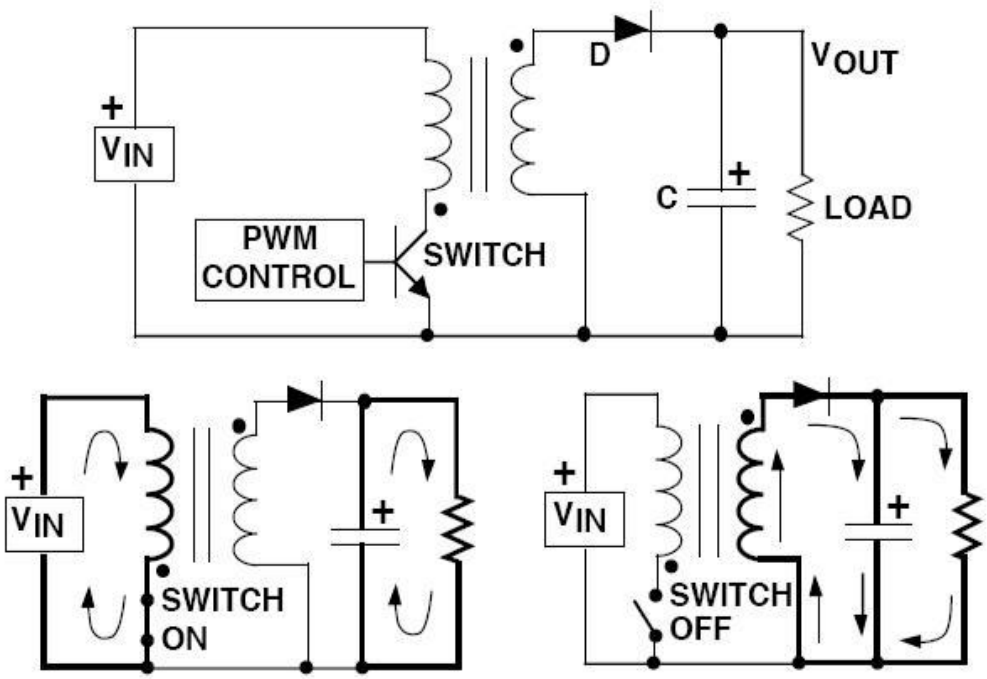
The Buck-Boost or Inverting regulator takes a DC input voltage and produces a DC output voltage that is opposite in polarity to the input. The negative output voltage can be either larger or smaller in magnitude than the input voltage. The Inverting regulator is shown in Figure.



When the switch is on, the input voltage is forced across the inductor, causing an increasing current flow through it. During the on time, the discharge of the output capacitor is the only source of load current. This requires that the charge lost from the output capacitor during the on time be replenished during the off time. When the switch turns off, the decreasing current flow in the inductor causes the voltage at the diode end to swing negative. This action turns on the diode, allowing the current in the inductor to supply both the output capacitor and the load. As shown, the load current is supplied by inductor when the switch is off, and by the output capacitor when the switch is on.

5.2.9 Flyback Regulator:

The Flyback is the most versatile of all the topologies, allowing the designer to create one or more output voltages, some of which may be opposite in polarity. Flyback converters have gained popularity in battery-powered systems, where a single voltage must be converted into the required system voltages (for example, +5V, +12V and -12V) with very high power conversion efficiency. The basic single-output flyback converter is shown in Figure.



The most important feature of the Flyback regulator is the transformer phasing, as shown by the dots on the primary and secondary windings. When the switch is on, the input voltage is forced across the transformer primary which causes an increasing flow of current through it.

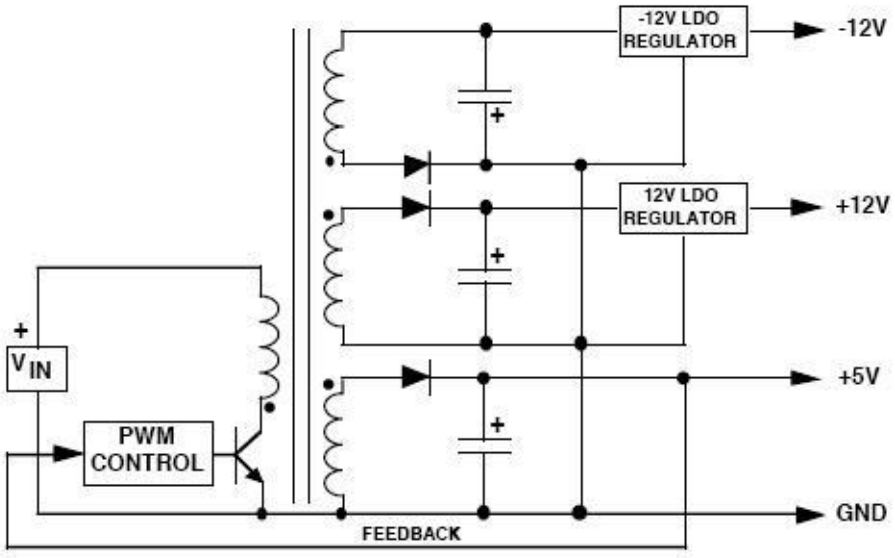
Note that the polarity of the voltage on the primary is dot-negative (more negative at the dotted end), causing a voltage with the same polarity to appear at the transformer secondary (the magnitude of the secondary voltage is set by the transformer seconday-to-primary turns ratio).

The dot-negative voltage appearing across the secondary winding turns off the diode, reventing current flow in the secondary winding during the switch on time. During this time, the load current must be supplied by the output capacitor alone. When the switch turns off, the decreasing current flow in the primary causes the voltage at the dot end to swing positive. At the same time, the primary voltage is reflected to the secondary with the same polarity. The dot-positive voltage

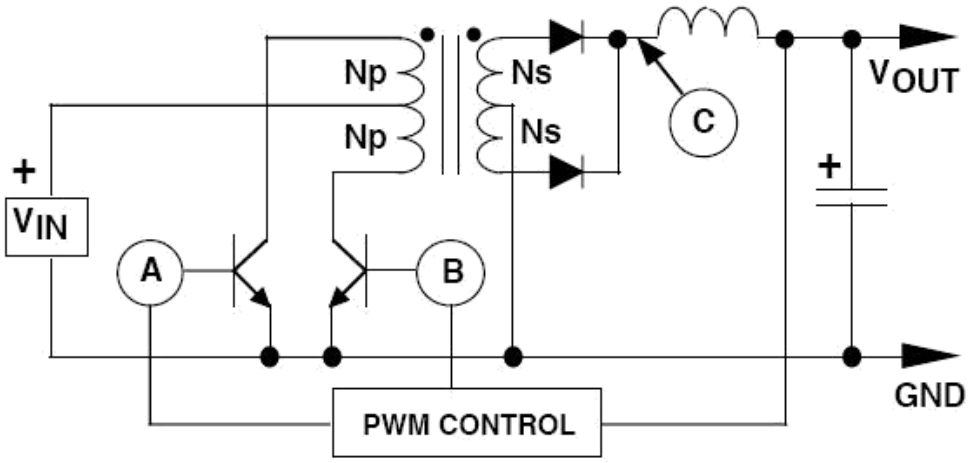
occurring across the secondary winding turns on the diode, allowing current to flow into both the load and the output capacitor. The output capacitor charge lost to the load during the switch on time is replenished during the switch off time. Flyback converters operate in either continuous mode (where the secondarycurrent is always >0) or discontinuous mode (where the secondary current falls to zero on each cycle).

5.2.10Generating Multiple Outputs:

Another big advantage of a Flyback is the capability of providing multiple outputs .In such applications, one of the outputs (usually the highest current) is selected to provide PWM feedback to the control loop, which means this output is directly regulated. The other secondary winding(s) are indirectly regulated, as their pulse widths will follow the regulated winding.The load regulation on the unregulated secondaries is not great (typically 5 - 10%), but is adequate for many applications. If tighter regulation is needed on the lower current secondaries, an LDO post-regulator is an excellent solution. The secondary voltage is set about 1V above the desired output voltage, and the LDO provides excellent output regulation withvery little loss of efficiency.



The Push-Pull converter uses two to transistors perform DC-DC conversion.The converter operates by turning on each transistor on alternate cycles (the two transistors are never on at the same time). Transformer secondary current flows at the same time as primary current (when either of the switches is on). For example, when transistor "A" is turned on, the input voltage is forced across the upper primary winding with dot-negative polarity. On the secondary side, a dot-negative voltage will appear across the winding which turns on the bottom diode.This allows current to flow into the inductor to supply both the output capacitor and the load. When transistor "B" is on, the input voltage is forced across the lower primary winding with dot-positive polarity.



The same voltage polarity on the secondary turns on the top diode, and current flows into the output capacitor and the load. An important characteristic of a Push-Pull converter is that the switch transistors have to be able the stand off more than twice the input voltage: when one transistor is on (and the input voltage is forced across one primary winding) the same magnitude voltage is induced across the other primary winding, but it is "floating" on top of the input voltage. This puts the collector of the turned-off transistor at twice the input voltage with respect to ground. The "double input voltage" rating requirement of the switch transistors means the Push-Pull converter is best suited for lower input voltage applications. It has been widely used in converters operating in 12V and 24V battery-powered systems.

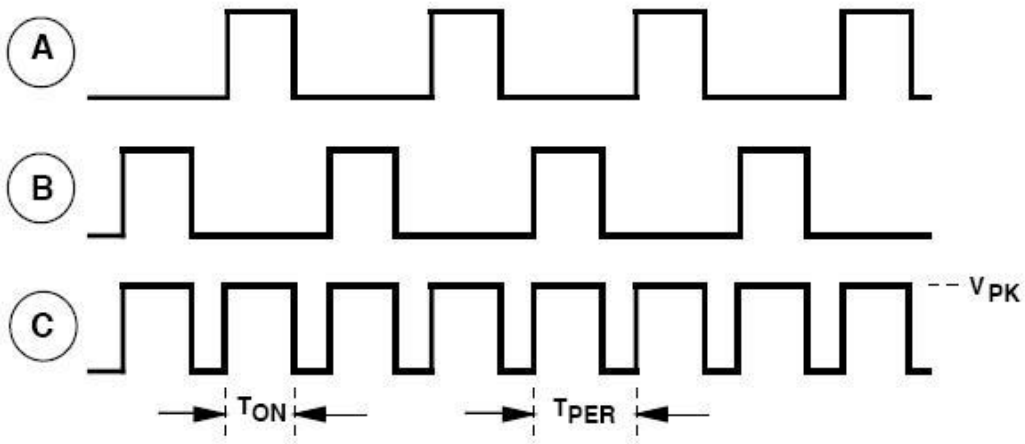
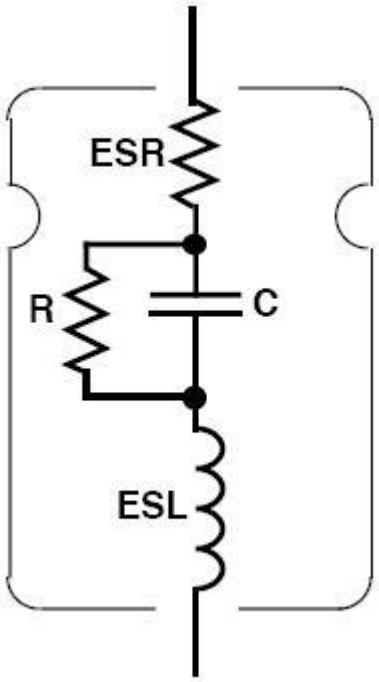


Figure shows a timing diagram which details the relationship of the input and output pulses. It is important to note that frequency of the secondary side voltage pulses is twice the frequency of

operation of the PWM controller driving the two transistors. For example, if the PWM control chip was set up to operate at 50 kHz on the primary side, the frequency of the secondary pulses would be 100 kHz. This highlights why the Push-Pull converter is well-suited for low voltage converters. The voltage forced across each primary winding (which provides the power for conversion) is the full input voltage minus only the saturation voltage of the switch. If MOS-FET power switches are used, the voltage drop across the switches can be made extremely small, resulting in very high utilization of the available input voltage. Another advantage of the Push-Pull converter is that it can also generate multiple output voltages (by adding more secondary windings), some of which may be negative in polarity. This allows a power supply operated from a single battery to provide all of the voltages necessary for system operation. A disadvantage of Push-Pull converters is that they require very good matching of the switch transistors to prevent unequal on times, since this will result in saturation of the transformer core (and failure of the converter).

Output Capacitor ESR effects:



The primary function of the output capacitor in a switching regulator is filtering. As the converter operates, current must flow into and out of the output filter capacitor. The ESR of the output capacitor directly affects the performance of the switching regulator. ESR is specified by the manufacturer on good quality capacitors, but be certain that it is specified at the frequency of intended operation.

General-purpose electrolytes usually only specify ESR at 120 Hz, but capacitors intended for high-frequency switching applications will have the ESR guaranteed at high frequency (like 20 kHz to 100 kHz). Some ESR dependent parameters are: Ripple Voltage: In most cases, the majority of the output ripples voltage results from the ESR of the output capacitor. If the ESR increases (as it will at low operating temperatures) the output ripple voltage will increase accordingly.

Efficiency: As the switching current flows into and out of the capacitor (through the ESR), power is dissipated internally. This "wasted" power reduces overall regulator efficiency, and can also cause the capacitor to fail if the ripple current exceeds the maximum allowable specification for the capacitor.

Loop Stability: The ESR of the output capacitor can affect regulator loop stability. Products such as the LM2575 and LM2577 are compensated for stability assumingthe ESR of the output capacitor will stay within a specified range. Keeping the ESR within the "stable" range is not always simple in designs that must operate over a wide temperature range. The ESR of a typical aluminum electrolytic may increase by 40X as the temperature drops from 25°C to -40°C.

In these cases, an aluminum electrolytic must be paralleled by another type ofcapacitor with a flatter ESR curve (like Tantalum or Film) so that the effective ESR (which is the parallel value of the two ESR's) stays within the allowable range. Note: if operation below -40°C is necessary, aluminum electrolytics are probably not feasible for use.

5.2.11 Bypass Capacitors:

High-frequency bypass capacitors are always recommended on the supply pins of IC devices, but if the devices are used in assemblies near switching converters bypass capacitors are absolutely required. The components which perform the high-speed switching (transistors and rectifiers) generate significant EMI that easily radiates into PC board traces and wire leads. To assure proper circuit operation, all IC supply pins must be bypassed to a clean, low-inductance ground.

5.2.12 LINEAR REGULATORS

- All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.
- Therefore the filters are used to obtain a —steady|| dc voltage from the pulsating one.
- The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.
- We know the combination of rectifier & filter can produce a dc voltage. But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an ac input or changes in the load current(I_L).
- The output of unregulated power supply is connected at the input of voltage regulator circuit.
- The voltage regulator is a specially designed circuit to keep the output voltage constant.
- It does not remain exactly constant. It changes slightly due to changes in certain parameters.

Factors affecting the output voltage:

i) I_L (Load Current)

ii) V_{IN} (Input Voltage)

iii) T (Temperature)

IC Voltage Regulators:

They are basically series regulators with all the basic blocks present inside the IC.

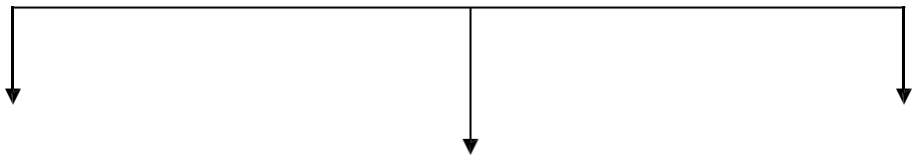
Therefore it is easier to use IC voltage regulator instead of discrete voltage regulators.

Important features of IC Regulators:

1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting
4. Thermal shutdown
5. Floating operation to facilitate higher voltage output

5.2.13 Classifications of IC voltage regulators:

IC Voltage Regulator



Fixed Volt Reg. Adjustable O/P Volt Reg Switching Reg

Positive/negative

- Fixed & Adjustable output Voltage Regulators are known as Linear Regulator.
- A series pass transistor is used and it operates always in its active

region. Switching Regulator:

1. Series Pass Transistor acts as a switch.
2. The amount of power dissipation in it decreases considerably.
3. Power saving result is higher efficiency compared to that of

linear. Adjustable Voltage Regulator:

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,

1. Adjustable output voltage from 1.2v to 57 v
2. Output current 0.10 to 1.5 A
3. Better load & line regulation
4. Improved overload protection
5. Improved reliability under the 100% thermal overloading

Adjustable Positive Voltage Regulator (LM317):

- LM317 series adjustable 3 terminal positive voltage regulator, the three terminals are Vin, Vout & adjustment (ADJ).
- LM317 requires only 2 external resistors to set the output voltage.
- LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as Vref.
- Vref (Reference Voltage) is a constant, hence current I1 flows through R1 will also be constant. Because resistor R1 sets current I1. It is called ―current set‖ or ―program resistor‖.

- Resistor R2 is called as ―Output set‖ resistors, hence current through this resistor is the sum of I1
- LM317 is designed in such as that Iadj is very small & constant with changes in line voltage & load current.
- The output voltage Vo is, Vo=R1I1+(I1+Iadj)R2---------- (1)

Where I1= Vref/R1

Vo =(Vref/R1)R1 + Vref/R1 + Iadj R2

= Vref + (Vref/R1)R2 + Iadj R2

Vo = Vref [1 + R2/R1] + Iadj R2---------- (2)

R1 = Current (I1) set resistor

R2 = output (Vo) set resistor

Vref = 1.25v which is a constant voltage between output and ADJ terminals.

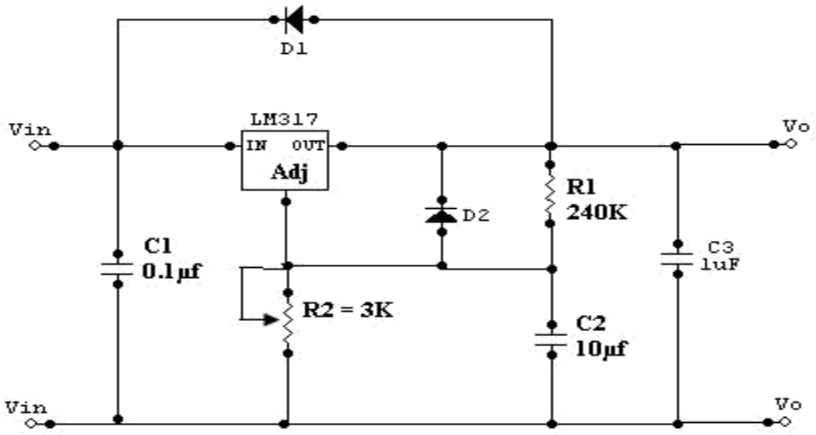
- Current Iadj is very small. Therefore the second term in (2) can be neglected.
- Thus the final expression for the output voltage is given by

Vo= 1.25v[1 + R2/R1]---------- (3)

Eqn (3) indicates that we can vary the output voltage by varying the resistance R2.

The value of R1 is normally kept constant at 240 ohms for all practical applications.

Practical Regulator using LM317:



- If LM317 is far away from the input power supply, then 0.1µf disc type or 1µf tantalum capacitor should be used at the input of LM317.
- The output capacitor Co is optional. Co should be in the range of 1 to 1000µf.
- The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple rejection ratio as high as 80 dB is obtainable at any output level.
- When the filter capacitor is used, it is necessary to use the protective diodes.
- These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.
- These diodes are required only for high output voltages (above 25v) & for higher values of output capacitance 25µf and above.

5.2.14 IC 723 – GENERAL PURPOSE REGULATOR

Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit protection
2. Output voltage is not adjustable These

limitations can be overcomes in IC723.

Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (I_{Lmax} = 150mA).
4. With the additional transistor used, I_{Lmax} upto 10A is obtainable.
5. Positive or Negative supply operation

6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

The simplified functional block diagram can be divided in to 4 blocks.

1. Reference generating block
2. Error Amplifier
3. Series Pass transistor
4. Circuitry to limit the current

1. Reference Generating block:

The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.

Fig: Functional block diagram of IC723

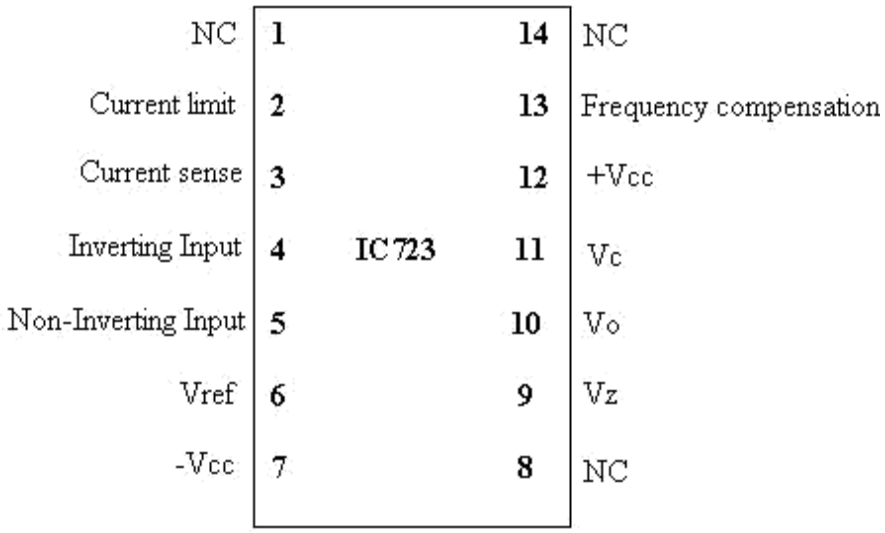


Fig : Pin diagram of IC723

3. Series Pass Transistor:

Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the I_L exceeds a predetermined limit.

- Low voltage , Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.

V_{load} = 2 to 7V

I_{load} = 150mA

5.2.15 IC723 as a LOW voltage LOW current :

Fig: Typical circuit connection diagram

- R1 & R2 from a potential divider between Vref & Gnd.
- The Voltage across R2 is connected to the Non – inverting terminal of the regulator IC

$$V_{non\text{-}inv} = \frac{R2}{R1+R2} V_{ref}$$

- Gain of the internal error amplifier is large

$$V_{non\text{-}inv} = V_{in}$$

- Therefore the Vo is connected to the Inverting terminal through R3 & R_{SC} must also be equal to $V_{non\text{-}inv}$

$$V_o = V_{non\text{-}inv} = \frac{R2}{R1+R2} V_{ref}$$

R1 & R2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

$$R3 = \frac{R1R2}{R+R2}$$

- Rsc (current sensing resistor) is connected between Cs & C_L. The voltage drop across Rsc is proportional to the I_L.
- This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.
- The current sourcing capacity is increased by including a transistor Q in the circuit.

- The output voltage , $V_o = \frac{R2}{R1+R2} V_{ref}$

5.2.16 IC723 as a HIGH voltage LOW Current:

Fig: Typical circuit connection diagram

- This circuit is capable of supplying a regulated output voltage between the range of 7 to 37 volts with a maximum load current of 150 mA.
- The Non – inverting terminal is now connected to Vref through resistance R3.
- The value of R1 & R2 are adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

$$\text{Vin} = \text{Vref} = \frac{R2}{R1 + R2}\ \text{Vo}$$

$$\text{Vo} = \frac{R1 + R2}{R2}\ \text{Vref}$$

Or

$$\text{Vo} = \left[1 + \frac{R1}{R2}\right]\ \text{Vref}$$

- Rsc is connected between C_L & Cs terminals as before & it provides the short circuit current limiting

$$Rsc = \frac{0.6}{ILimit}$$

- The value of resistors R3 is given by ,

$$R3 = R1 \text{ ll } R2 = \frac{R1R2}{R+R2}$$

IC723 as a HIGH voltage HIGH Current:

Fig: Typical circuit connection diagram

- An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.
- For this circuit the output voltage varies between 7 & 37V.
- Transistor Q increase the current sourcing capacity thus $I_{L(MAX)}$ ia greater than 150mA.
- The output voltage Vo is given by ,

$$Vo = \left(\frac{R1 + R2}{R2} \right) Vref$$

- The value of Rsc is given by $Rsc = \frac{0.6}{ILimit}$

5.3.1 SWITCHING REGULATOR:

An example of general purpose regulator is Motorola's MC1723. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.

To minimize the power dissipation during switching, the external transistor used must be a switching power transistor.

To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.

- A regulator constructed to operate in this manner is called a series switching regulator. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.
- This output is filtered through a low pass LC filter to produce an average dc output voltage.
- Thus the output voltage is proportional to the pulse width and frequency.

- The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%

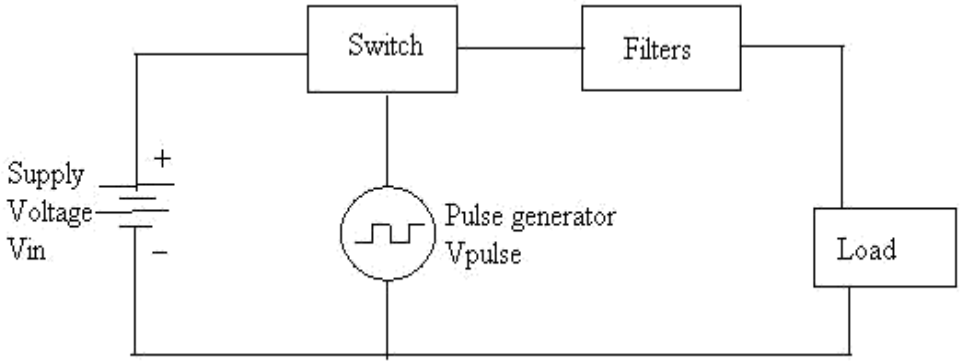


Fig : Basic Switching regulator

A basic switching regulator consists of 4 major components,

1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

1. Voltage Source Vin:

It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

- It must supply the required output power & the losses associated with the switching regulator.

- It must be large enough to supply sufficient dynamic range for line & load regulations.
- It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.
- It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode. The pulse generator output alternately turns the switch ON & OFF

3. Pulse generator Vpulse:

It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively. The most effective frequency range for the pulse generator for optimum efficiency 20 KHz. This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

- The duty cucly of the pulse wave form determines the relationship between the input & output voltages. The duty cycle is the ratio of the on time ton, to the period T of the pulse waveform.

Duty cycle = ————

ton ton + toff

$$= \frac{ton}{T} = \text{ton f.}$$

Where ton = On-time of the pulse waveform

toff=off-time of the pulse wave form

T = time period = ton + toff

= 1/frequency or

T = 1/f

- Typical operating frequencies of switching regulator range from 10 to 50khz.
- Lower operating frequency improve efficiency & reduce electrical noise, but require large filter components (inductors & capacitors).

4. Filter F1:

It converts the pulse waveform from the output of the switch into a dc voltage. Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.

The output voltage Vo of the switching regulator is a function of duty cycle & the input voltage Vin.

Vo is expressed as follows,

$$Vo = \frac{ton}{T} Vin$$

- This equation indicates that, if time period T is constant, Vo is directly proportional to the ON-time, ton for a given value of Vin. This method of changing the output voltage by varying ton is referred to as a pulse width modulation.
- Similarly, if ton is held constant, the output voltage Vo is inversely proportional to the period T or directly proportional to the frequency of the pulse waveform. This method of varying the output voltage is referred to as frequency modulation (FM).
- Switching regulator can operate in any of 3 modes

i) Step – Down

ii) Step – Up

iii) Polarity inverting

5.3.2 POWER AUDIO AMPLIFIER IC LM380:

Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centring to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac coupled.
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedence.
8. Low total harmonic distortion
9. Bandwidth of 100KHz at Pout = 2W & $R_L = 8\Omega$

Introduction:

Small signal amplifier are essentially voltage amplifier that supply their loads with larger amplifier signal voltage. On the other hand , large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors. In audio applications, however, the amplifier called upon to deliver much higher current than that suppkied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose opo-amps.

However there are two possible solutions,

- To use discrete or monolithic power transistors called power boosters at the output of the op-amp
- To use specialized ICs designed as power amplifiers.

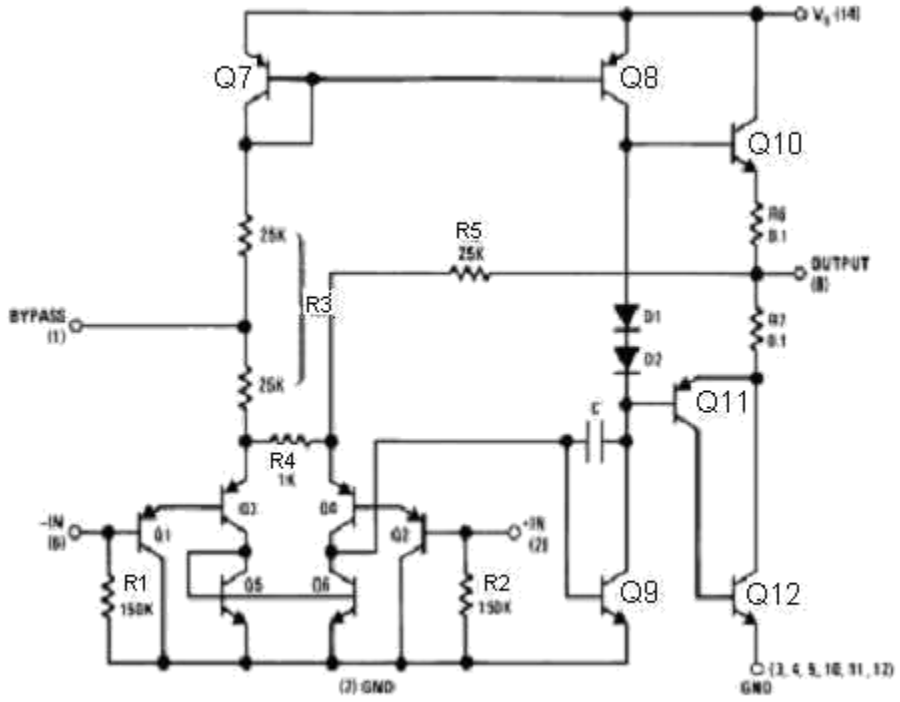


Fig : Functional block diagram of Audio Power Amplifier

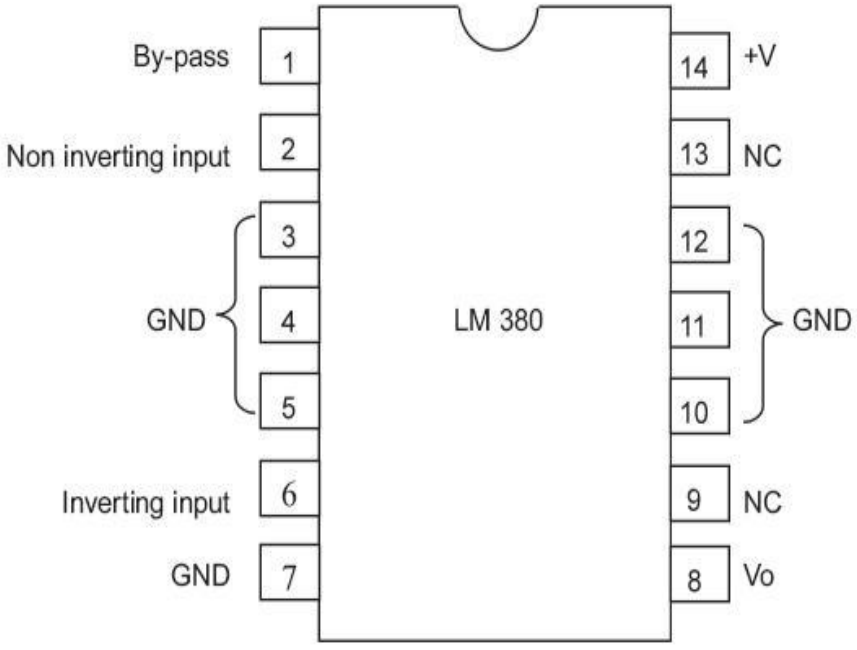


Fig: Pin diagram

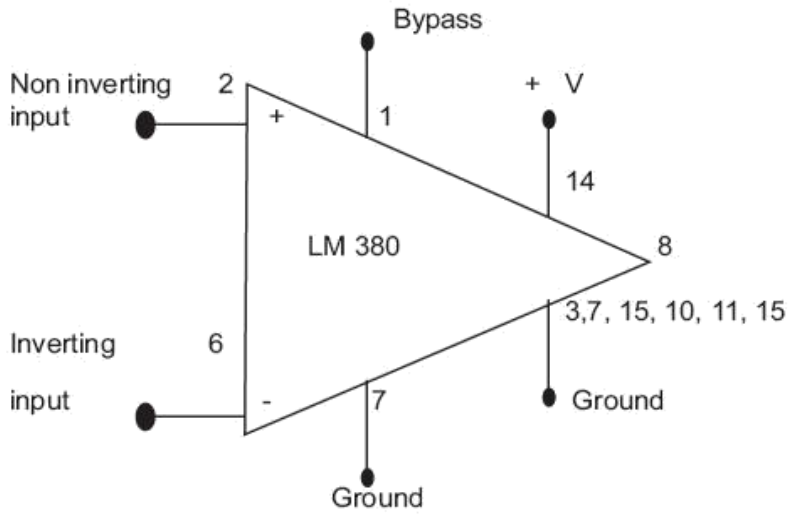


Fig : Block diagra

LM380 circuit description:

It is connected of 4 stages,

- **(i)** PNP emitter follower
- **(ii)** Different amplifier
- **(iii)** Common emitter
- **(iv)** Emitter follower

(i) PNP Emitter follower:

- The input stage is emitter follower composed of PNP transistors Q1 & Q2 which drives the PNP Q3-Q4 differential pair.
- The choice of PNP input transistors Q1 & Q2 allows the input to be referenced to ground i.e., the input can be direct coupled to either the inverting & non-inverting terminals of the amplifier.

(ii) Differential Amplifier:

- The current in the PNP differential pair Q3-Q4 is established by Q7, R3 & +V.
- The current mirror formed by transistor Q7, Q8 & associated resistors then establishes the collector current of Q9.

- Transistor Q5 & Q6 constitute of collector loads for the PNP differential pair.
- The output of the differential amplifier is taken at the junction of Q4 & Q6 transistors & is applied as an input to the common emitter voltage gain.

(iii) Common Emitter:

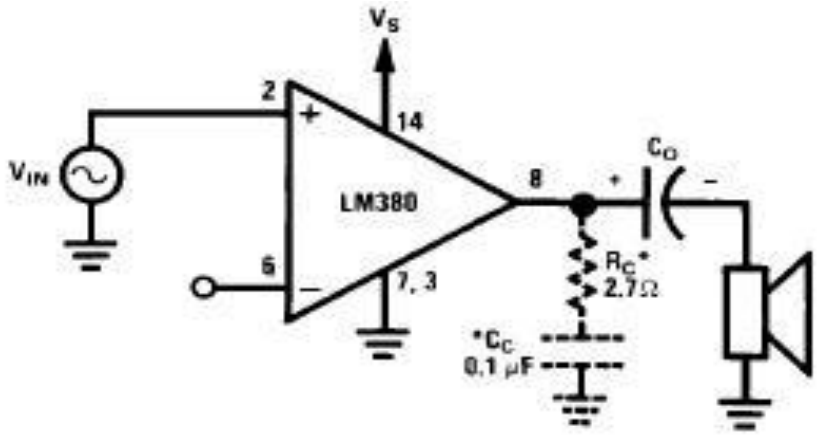
- Common Emitter amplifier stage is formed by transistor Q9 with D1, D2 & Q8 as a current source load.
- The capacitor C between the base & collector of Q9 provides internal compensation & helps to establish the upper cutoff frequency of 100 KHz.
- Since Q7 & Q8 form a current mirror, the current through D1 & D2 is approximately the same as the current through R3.
- D1 & D2 are temperature compensating diodes for transistors Q10 & Q11 in that D1 & D2 have the same characteristics as the base-emitter junctions of Q11. Therefore the current through Q10 & (Q11-Q12) is approximately equal to the current through diodes D1 & D2.

(iv) (Output stage) - Emitter follower:

- Emitter follower formed by NPN transistor Q10 & Q11. The combination of PNP transistor Q11 & NPN transistor Q12 has the power capability of an NPN transistors but the characteristics of a PNP transistor.
- The negative dc feedback applied through R5 balances the differential amplifier so that the dc output voltage is stabilized at +V/2;
- To decouple the input stage from the supply voltage +V, by pass capacitor in order of micro farad should be connected between the by pass terminal (pin 1) & ground (pin 7).
- The overall internal gain of the amplifier is fixed at 50. However gain can be increased by using positive feedback.

5.4.1 APPLICATIONS:

(i) Audio Power Amplifier:



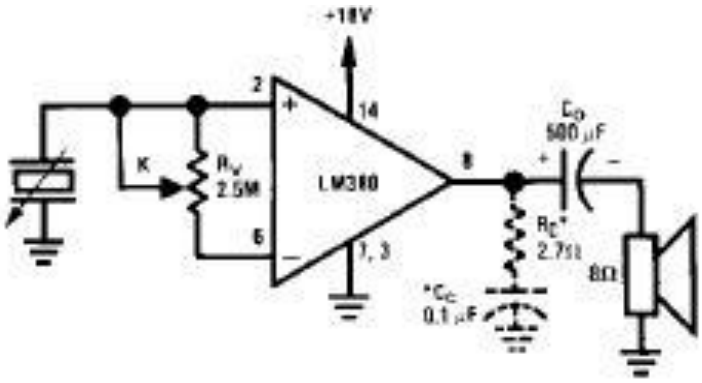
- Amplifier requires very few external components because of the internal biasing, compensation & fixed gain.
- When the power amplifier is used in the non inverting configuration, the inverting terminal may be either shorted to ground, connected to ground through resistors & capacitors.
- Similarly when the power amplifier is used in the inverting mode, the non inverting terminal may be either shorted to ground or returned to ground through resistor or capacitor.
- Usually a capacitor is connected between the inverting terminal & ground if the input has a high internal impedance.
- As a precautionary measure, an RC combination should be used at the output terminal (pin 8) to eliminate 5-to-10 MHz oscillation.
- C1 is coupling capacitor which couples the output of the amplifier to the 8 ohms loud speaker which act as a load. The amplifier will amplify the V_{in} applied at the non-inverting terminal.

(ii) LM 380 as a High gain:

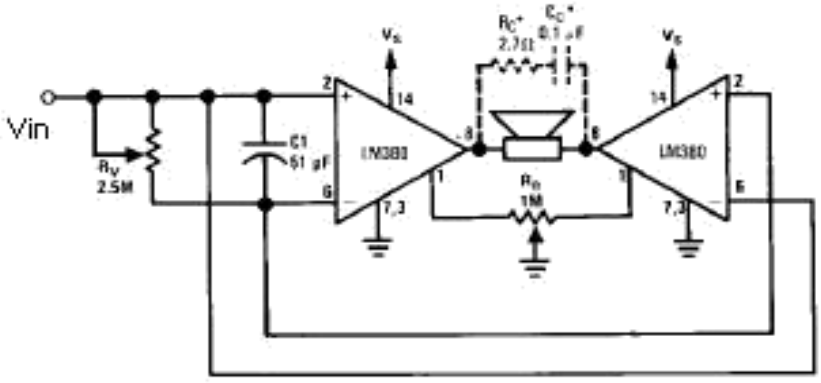
- The gain of LM380 is internally fixed at 50. But it can be increased by using the external components.
- The increase in gain is possible due to the use of positive feedback, this setup to obtain a gain 200.

(iii) LM 380 as a variable Gain:

- Instead of getting a fixed gain of 50, it is possible to obtain a variable gain up to 50 by connecting a potentiometer between the input terminals.



(iv) LM 380 as a Bridge Audio Power Amplifier:



- If a certain application requires more power than what is provided by a single LM380 amplifier, then 2 LM380 chips can be used in the bridge configuration.
- With this arrangement we get an output voltage swing which is twice that of a single LM380 amplifier.
- As the voltage is doubled, power output will increase by four times that of a single LM380 amplifier. The pot R4 is used to balance the output offset voltages of the two chips.

(v) Intercom system using LM 380:

- When the switch is in Talk mode position, the master speaker acts as a microphone.
- When the switch is in Listen position, the remote speaker acts as a microphone.
- In either phone the overall gain of the circuit is the same depends on the turns of transformer T.

Fig: Talk mode

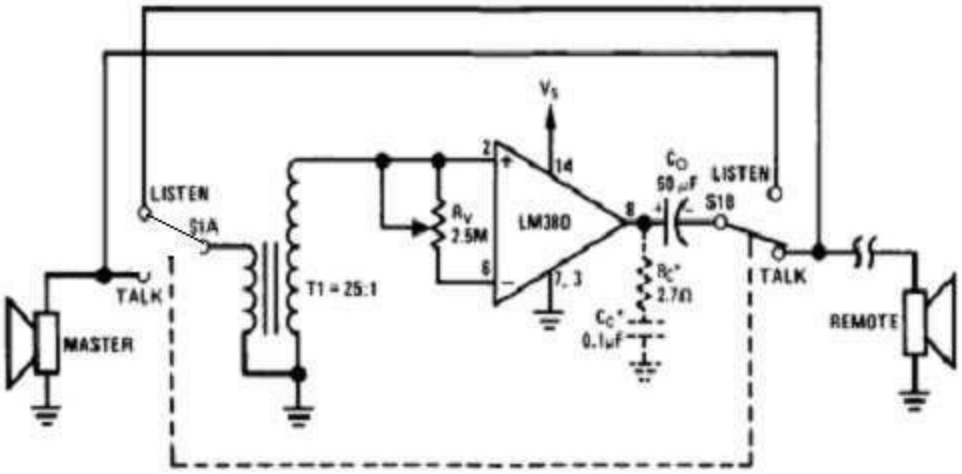


Fig: Listen mode

5.5.1 OPTOCOUPLERS/OPTOISOLATORS:

- Optocouplers or Optoisolators is a combination of light source & light detector in the same package.
- They are used to couple signal from one point to other optically, by providing a completer electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.
- Depending on the type of light source & detector used we can get a variety of optocouplers.

They are as follows,

(i) LED – LDR optocoupler

(ii) LED – Photodiode optocoupler

(iii) LED – Phototransistor optocoupler

Characteristics of optocoupler:

(i) Current Transfer Ratio(CTR)

(ii) Isolation Voltage

(iii) Response Time

(iv) Common Mode Rejection

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the input forward current (If)

$$CTR = Ic/If * 100\%$$

Its value depends on the devices used as source detector. (ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii)Response Time:

Response time indicates how fast an optocoupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

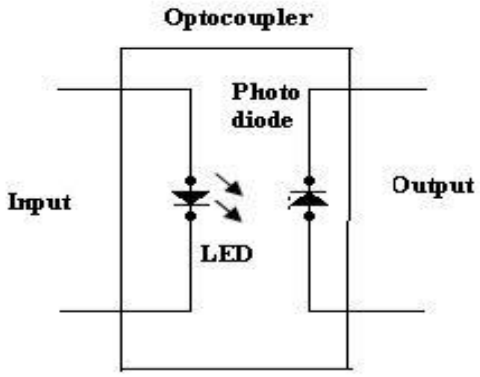
(iv)Common mode Rejection:

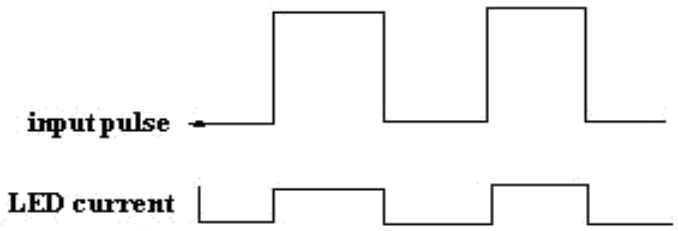
Eventhough the optocouplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement

current Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allow the noise to appear in the output.

Types of optocoupler:

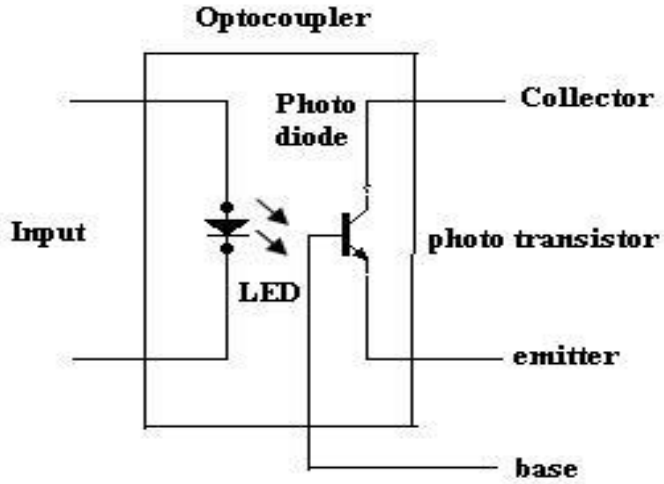
(i) LED – Photodiode optocoupler:

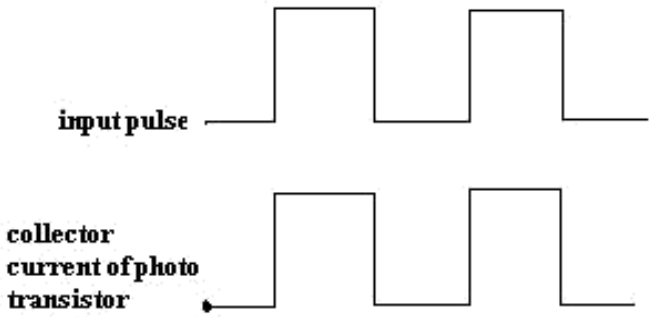




- LED photodiode shown in figure, here the infrared LED acts as a light source & photodiode is used as a detector.
- The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode.
- In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

(ii) LED – Phototransistor Optocoupler:





- The LED phototransistor optocoupler shown in figure. An infrared LED acts as a light source and the phototransistor acts as a photo detector.
- This is the most popularly used optocoupler, because it does not need any additional amplification.
- When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.
- In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.
- The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.

Advantages of Optocoupler:

- Control circuits are well protected due to electrical isolation.
- Wideband signal transmission is possible.
- Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- Interfacing with logic circuits is easily possible.
- It is small size & light weight device.

Disadvantages:

- Slow speed.

- Possibility of signal coupling for high power signals.

Applications:

Optocouplers are used basically to isolate low power circuits from high power circuits.

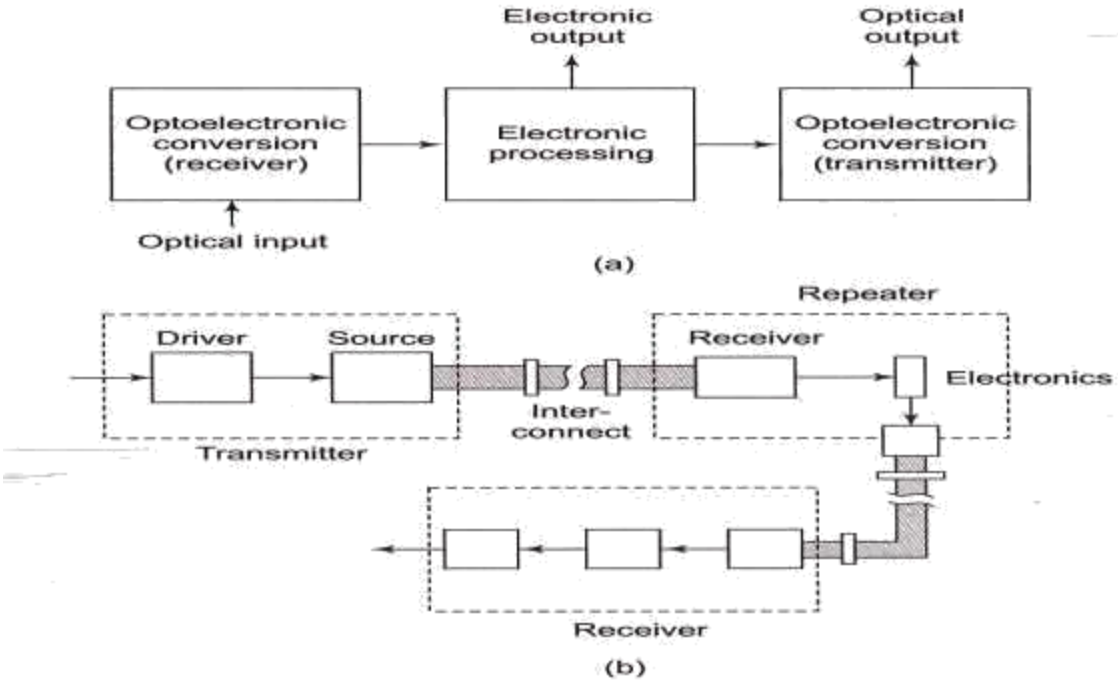
- At the same time the control signals are coupled from the control circuits to the high power circuits.
- Some of such applications are,
  - (i) AC to DC converters used for DC motor speed control
  - (ii) High power choppers
  - (iii) High power inverters
- One of the most important applications of an optocoupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.

- Note that the input & output waveforms are 180º out of phase as the output is taken at the collector of the phototransistor.

5.5.2 Optocoupler IC:

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.

- This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.
- The infrared radiation from the LED gets focused on the internal phototransistor.
- The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.
- The block diagram shows the opto-electronic-integrated ciruit (OEIC) and the major components of a fiber-optic communication facility.



1.Define an Integrated circuit.

An integrated circuit(IC) is a miniature ,low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon.The active components are transistors and diodes and passive components are resistors and capacitors.

2.What are the basic processes involved in fabricating ICs using planar technology?

1.Silicon wafer (substrate) preparation
2.Epitaxial growth
3.Oxidation
4.Photolithography
5.Diffusion
6.Ion implantation
7.Isolation technique
8.Metallization
9.Assembly processing & packaging

3.List out the steps used in the preparation of Si – wafers.

1.Crystal growth &doping
2.Ingot trimming & grinding
3.Ingot slicing
4.Wafer policing & etching
5.Wafer cleaning

4.Write the basic chemical reaction in the epitaxial growth process of pure silicon.

The basic chemical reaction in the epitaxial growth process of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$SiCl_4 + 2H_2 \xrightarrow{1200^oC} Si + 4\,HCl$$

6.What are the two important properties of SiO_2?

1.SiO_2 is an extremely hard protective coatng & is unaffected by almost all reagents except by hydrochloric acid. Thus it stands against any contamination.

2.By selective etching of SiO_2 , diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

7.Explain the process of oxidation.

The silicon wafers are stacked up in a quartz boat & then inserted into quartz furnace tube. The Si wafers are raised to a high temperature in the range of 950 to 1150^oC & at the same time, exposed to a gas containing O_2 or H_2O or both.The chemical action is

$Si + 2H_2O$ ••••••••••> $Si\ O_2 + 2H_2$

8. What are oxidation induced defects in semi conductor? 1.Stacking faults

2.Oxide isolation defects

Stacking faults:

Structural defects in the silicon lattice is called oxidation induced stacking faults.The growth of stacking faults is a strong function of substrate orientation , conductivity type & defect nuclei present.The stacking faults formation can be suppressed by the addition of HCl.

Oxide isolation defects :

The stress along the edges of an oxidised area produce severe damage in the silicon. Such defects results in increased leakage in nearby devices.High temperatures (around 950^oC) will prevent stress induced defect formation.

9.What is lithography?

Lithography is a process bywhich the pattern appearing on the mask is transfered to the wafer.It involves two steps: the first step requires applying a few drops of photoresist to the surface of the wafer & the second step is spinning the surface to get an even coating of the photoresist across the surface of the wafer.

10.What are the different types of lithography? What is optical lithography?

The different types of lithography are :

1.Photolithography
2.Electron beam lithography
3.X ray beam lithography
4.Ion beam lithography

Optical lithography:

Optical lithography comprises the formation images with visible or UV radiation in a photoresist using contact, proximity or projection printing.

13.What are the two processes involved in photolithography?

a) Making a photographic mask b) Photoetching

The development of photographic mask involves the preparation of initial artwork and its reduction , decomposition of initial artwork or layout into several mask layers. Photoetching is used for the removal of SiO_2 from desired regions sothat the desired impurities can be diffused.

14.Distinguish between dry etching & wet etching.

Dry etching	Wet etching
1.Gaseous mixture is used as the chemical reagent.	Chemical reagents used are in the liquid form.
2.Smaller line openings(1µm) are possible with dry etching	Line opening are larger.(> 1µm)
3.It produces straight walled etching process.	It produces patterns with undercutting.

15.What is meant by reactive plasma etching?

The term reactive plasma is meant to describe a discharge in which ionization & fragmentation of gases takesplace& produce chemically active plasma species, frequently oxidizers and reducing agents.Such plasmas are reactive both in the gas phase & with solid surfaces exposed to them.When these interactions are used to form volitile products so that material is removed or etching of material form surfaces that are not masked to form lithographic patterns , the technique is known as reactive plasma etching.

16.What are isotropic & anisotropic etching processes?

Isotropic etching is a wet etching process which involves undercutting.

Aisotropic etching is a dry etching process which provides straight walled patterns.

17.Define diffusion.

The process of introducing impurities into selected regions of a silicon wafer is called diffusion. The rate atwhich various impurities diffuse into the silicon will be of the order of 1µm/hr at the temperature range of 900^{o}C to 1100^{o}C .The impurity atoms have the tendency to move from regions of higher concentrations to lower concentrations.

18.What is dielectric isolation?

In dielectric isolation, a layer of solid idelectric such as SiO_2 or ruby completely surrounds each components thereby producing isolation , both eletrical & physical.This isolating dielectric layer is thick enough so that its associated capacitance is negligible.Also, it is possible to fabricate both pnp & npn transistors within the same silicon substrate.

19.What are the advantages of ion implantation technique?

1. It is performed at low temperature.Therefore, previously diffused regions have a lesser tendency for lateral spreading.
2. In diffusion process, temperature has to be controlled over a large area inside the oven, wheras in ion implantation process,accelerating potential & beam content are dielectrically controlled from outside.

20.What is metallization?

The process of producing a thin metal film layar that will serve to make interconnection of the various components on the chip is called metallization.

UNIT II
Characteristics of Op-Amp

1.What are the advantages of ICs over discrete circuits.?

1. Minimization & hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability

4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds
7. Reduction in power consumption

2. What is OPAMP?

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers , followed by a level translator and an output stage.It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathamatical functions such as addition, subtraction , multiplication, integration & differentiation

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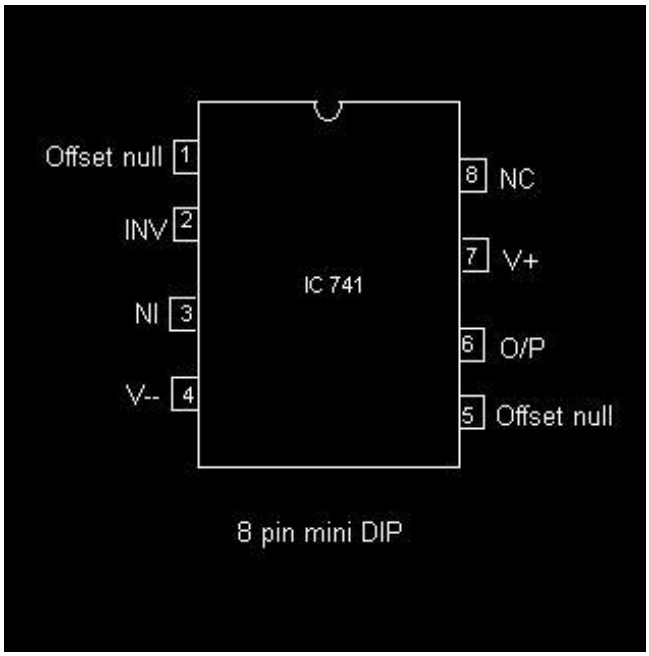
3.Draw the pin configuration of IC741.



4. List out the ideal characteristics of OPAMP?

(i)Open loop gain infinite
(ii)Input impedance infinite
(iii)Output impedance low
(iv)Bandwidth infinite
(v)Zero offset,ie,Vo=0 when V1=V2=0

5.what are the different kinds of packages of IC741?

a)Metal can (TO) package
b)Dual- in- line package
c)Flat package or flat pack

6.What are the assumptions made from ideal opamp characteristics?

i)The current drawn by either of the input terminals(non-inverting/inverting) is negligible.

ii)the potential difference between the inverting & non- inverting

input terminals is zero.

7. Mention some of the linear applications of op – amps :

Adder, subtractor, voltage –to- current converter, current –to- voltage converters, instrumentation amplifier, analog computation ,power amplifier, etc are some of the linear op-amp circuits.

8.Mention some of the non – linear applications of op-amps:-

Rectifier, peak detector, clipper, clamper, sample and hold circuit, log amplifier, anti –log amplifier, multiplier are some of the non – linear op-amp circuits.

9.What are the areas of application of non- linear op- amp circuits?

- industrial instrumentation
- Communication
- Signal processing

10.What happens when the common terminal of V^+ and V^- sources is not grounded?

If the common point of the two supplies is not grounded, twice the supply voltage will get applied and it may damage the op-amp.

11.Define input offset voltage.

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage.

12. Define input offset current. State the reasons for the offset currents at the input of the op-amp.

The difference between the bias currents at the input terminals of the op-amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors.Since the input transistors cannot be made identical,there exists a difference in bias currents.

13. Define CMRR of an op-amp.

The relative sensitivity of an op-amp to a difference signal as compared to a common –mode signal is called the common –mode rejection ratio. It is expressed in decibels.

$$CMRR = A_d/A_c$$

14.In practical op-amps, what is the effect of high frequency on its performance?

The open- loop gain of op-amp decreases at higher frequencies due to the presence of parasitic capacitance. The closed- loop gain increases at higher frequencies and leads to instability.

15. What is the need for frequency compensation in practical op-amps?

Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability.

16.Mention the frequency compensation methods.

*Dominant-pole compensation

*Pole- zero compensation.

17.What are the merits and demerits of Dominant-pole compensation?

*noise immunity of the system is improved.

*Open-loop bandwidth is reduced.

18.Define slew rate**.**

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage.An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage.

19.Why IC 741 is not used for high frequency applications?

IC741 has a low slew rate because of the predominance of capacitance present in the circuit at higher frequencies. As frequency increases the output gets distorted due to limited slew rate.

20.What causes slew rate?

There is a capacitor with- in or outside of an op-amp to prevent oscillation.It is this capacitor which prevents the output voltage from responding immediately to a fast changing input.

21.Define thermal drift.

The bias current , offset current & offset voltage change with temperature. A circuit carefully nulled at 25^{o}C may not remain so when the temperature raises to 35^{o}C.This is called thermal drift . Often, offset current drift is expressed in nA/ ^{o} C and offset voltage drift in mV/ ^{o}C.

22.Define supply voltage rejection ratio(SVRR)

The change in OPAMP's input offset voltage due to variations in supply voltage is called the supply voltage rejection ratio.It is also called Power Supply Rejection Ratio(PSRR) or Power Supply Sensitivity(PSS).

UNIT III
Applications of Op Amp

1.What is the need for an instrumentation amplifier?

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

2.List the features of instrumentation amplifier:

- high gain accuracy
- high CMRR
- high gain stability with low temperature co-efficient
- low dc offset
- low output impedance

3.What is a comparator?

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is an open loop op - amp with output + Vsat .

4.What are the applications of comparator?

- Zero crossing detector
- Window detector
- Time marker generator
- Phase detector

5.What is a Schmitt trigger?

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform.

6.What is a multivibrator?

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator.

7.What do you mean by monostable multivibrator?

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi-stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state.

8.What is an astable multivibrator?

Astable multivibrator is a free running oscillator having two quasi-stable states. Thus, there is oscillations between these two states and no external s i g n a l a r e required to produce the change in state.

9.What is a bistable multivibrator?

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied . Thus, it requires two external triggers before it returns to its initial state

10.What are the requirements for producing sustained oscillations in feedback

circuits? For sustained oscillations,

– The total phase shift around the loop must be zero at the desired frequency of oscillation, fo. ie, LAB =0 (or) 360°

– At fo, the magnitude of the loop gain | A b | should be equal to unity

11.What are the different types of filters?

Based on functions: Low pass filter,High pass filter,Band pass filter, Band reject filter

Based on order of transfer function: first ,second,third higher order filters.

Based on configuration: Bessel,Chebychev,Butterworth filters.

12.List the broad classification of ADCs.

1. Direct type ADC.
2. Integrating type ADC.

13.List out the direct type ADCs.

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter
4. Successive approximation type converter

14. List out some integrating type converters.

1. Charge balancing ADC
2. Dual slope ADC

15.What is integrating type converter?

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter.

16.Explain in brief the principle of operation of successive Approximation ADC.

The circuit of successive approximation ADC consists of a successive approximation register (SAR), to find the required value of each bit by trial & error.With the arrival of START command, SAR sets the MSB bit to 1. The O/P is converted into an analog signal & it is compared with I/P signal. This O/P is low or High. This process continues until all bits are checked.

17.What are the main advantages of integrating type ADCs?

i. The integrating type of ADC's do not need a sample/Hold circuit at the input.
ii. It is possible to transmit frequency even in noisy environment or in an isolated form.

18.Define conversion time.

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used & the propagation delay of circuit components.

The conversion time of a successive approximation type ADC is given by T(n+1)

where T---clock period

Tc---conversion time

n----no. of bits

19.Define resolution of a data converter.

The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter.

Resolution (in volts)= VFS/2^n-1=1 LSB increment. The resolution of an ADC is defined as the smallest change in analog input for a one-bit change at the output.

20.Explain in brief stability of a converter:

The performance of converter changes with temperature age & power supply variation. So all the relevant parameters such as offset, gain, linearity error & monotonicity must be specified over the full temperature & power supply ranges to have better stability performances.

21.What is meant by linearity?

The linearity of an ADC/DAC is an important measure of its accuracy & tells us how close the converter output is to its ideal transfer characteristics. The linearity error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ±½LSB.

22.What is a sample and hold circuit? Where it is used?

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

23.Define sample period and hold period.

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period.The time period during which the voltage across the capacitor is held constant is called hold period.

UNIT IV
Special ICs

1.What are the applications of 555 Timer ?

- astable multivibrator
- monostable multivibrator
- Missing pulse detector
- Linear ramp generator
- Frequency divider
- Pulse width modulation
- FSK generator
- Pulse position modulator
- Schmitt trigger

2.List the applications of 555 timer in monostable mode of operation:

*missing pulse detector
*Linear ramp generator
*Frequency divider
*Pulse width modulation.

3. List the applications of 555 timer in Astable mode of operation: *FSK generator
*Pulse-position modulator

4.Define 555 IC?

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions.

5.List the basic blocks of IC 555 timer?

- A relaxation oscillator
- RS flip flop
- Two comparator
- Discharge transistor.

.

6.List the features of 555 Timer?

- It has two basic operating modes: monostable and astble
- It is available in three packages. 8 pin metal can , 8 pin dip, 14 pin dip.
- It has very high temperature stability.

7.Define duty cycle?

The ratio of high output and low output period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON Time to total time.

8.Define VCO.

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.

9.List the features of 566 VCO.

- Wide supply voltage range(10-24V)
- Very linear modulation characteristics
- High temperature stability

10. What do u mean by PLL?

A PLL is a basically a closed loop system designed to lock output frequency and phase to the frequency and phase of an input signal.

11. Define lock range.

When PLL is in lock, it can trap freq changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called as lock range.

12. Define capture range.

The range of frequencies over which the PLL can acquire lock with the input signal is called as capture range.

13. Define pull- in time.

The total time taken by the PLL to establish lock is called pull- in time.

14. List the applications of 565 PLL.

- Frequency multiplier
- Frequency synthesizer
- FM detector

15. What are the two types of analog multiplier Ics?

a) IC AD 533
b) IC AD 534

16. What is ICAD 533?

It is a multiplier IC by analog devices. It is a low cost IC comprising a transconductance multiplying element, stable reference and an output amplifier.

17. List the features of ICAD533.

- Its operation is very simple.
- Only 4 external adjustments are necessary
- Maximum 4 quadrant error is below 0.5%

18. What is ICAD 534?

It is a multiplier IC by analog devices. It is the first general purpose multiplier capable of providing gain upto X100.

19. List the features of ICAD534.

- Adjustable scale factor
- Low noise
- Excellent long time stability

20. List the few applications of ICAD534.

- Multiplier
- Divider
- High quality signal processing

UNIT V
Application ICs

1.What is a voltage regulator?

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

2.Give the classification of voltage regulators:

*Series / Linear regulators
*Switching regulators.

3.What is a linear voltage regulator?

Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region .The output voltage is controlled by the continous voltage drop taking place across the series pass transistor.

4.What is a switching regulator?

Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continously.This gives improved efficiency over series regulators.

5.What are the advantages of IC voltage regulators?

*low cost
*high reliability
*reduction in size
*excellent performance

6.Give some examples of monolithic IC voltage regulators:

78XX series fixed output, positive voltage regulators
79XX series fixed output, negative voltage regulators
723 general purpose regulator.

7.What is the purpose of having input and output capacitors in three terminal IC regulators?

A capacitor connected between the input terminal and ground cancels the inductive effects due to long distribution leads. The output capacitor improves the transient response.

8. Define line regulation.

Line regulation is defined as the percentage change in the output voltage for a change in the input voltage.It is expressed in millivolts or as a percentage of the output

9.Define load regulation.

Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.

10.What is meant by current limiting?

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

11.Give the drawbacks of linear regulators:

*The input step down transformer is bulky and expensive because of low line frequency.

*Because of low line frequency,large values of filter capacitors are required to decrease the ripple.

*Efficiency is reduced due to the continous power dissipation by the transistor as it operates in the linear region.

12.What is the advantage of switching regulators?

*Greater efficiency is achieved as the power transistor is made to operate as low impedance switch.Power transmitted across the transistor is in discrete pulses rather than as a steady current flow.

*By using suitable switching loss reduction technique, the switching frequency can be increased so as to reduce the size and weight of the inductors and capacitors.

13.What is an opto-coupler IC?

Opto-coupler IC is a combined package of a photo-emitting device and a photo-sensing device.

14.What are the types of optocouplers?

- LED and a photo diode,
- LED and photo transistor,
- LED and Darlington.
-

15.Give two examples of IC optocouplers?

Examples for opto-coupler IC

- MCT 2F
- MCT 2E .

16. Mention the advantages of opto-couplers:

*Better isolation between the two stages.

*Impedance problem between the stages is eliminated. *Wide frequency response.

*Easily interfaced with digital circuit.

*Compact and light weight.
*Problems such as noise, transients, contact bounce,.. are eliminated.

17.What is an isolation amplifier?

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

18.What are the features of isolation amplifier?

- Easy to use
- Ultra low leakage
- 18 pin DIP package

19. What is LM380?

It is a power amplifier produced by national semiconductor.It is capable of delivering 2.5 W min, to 8 ohm load.

20.What are the features of MA78s40?

- Step up,step down or inverting operation
- Operation from 2.5 to 40 V.
- 80Db line and load regu